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Taran V. Harman for the degree of Master of Science in

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The long-term goal of the research project initiated with this thesis is the development of lead-free, fully-transparent ferroelectric devices, such as ferroelectric capacitors or ferroelectric-gate field-effect transistors. Ferroelectric materials exhibit spontaneous polarization with the application of an external electric field, which is persistent upon removal of the applied field, and can be reversed by applying a field of opposite polarity. Ferroelectric thin films can be used in non-volatile memory applications in storage capacitors or as the gate dielectric of a field-effect transistor. Ferroelectric devices are fabricated by the deposition of ferroelectric lead zirconate titanate (PZT) by RF sputtering and by the chemical solution deposition (CSD) method of spin coating. Ferroelectric PZT capacitors are characterized by measuring capacitance and conductance as a function of frequency, and by measuring polarization as a function of applied electric field using a Sawyer-Tower circuit. Ferroelectric PZT capacitors with opaque Au or Ni top electrodes exhibit dielectric constants in the range of ∼300-600, typical of a ferroelectric film. However, all attempts to fabricate ferroelectric capacitors with transparent top contacts, involving several types of transparent conductors and the use of insulating buffer layers, resulted in charge injection and breakdown before the ferroelectric layer is fully polarized.

Ferroelectric Thin Film Development

by

Taran V. Harman

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1. INTRODUCTION

The first observation of ferroelectricity was made in 1920 when Valasek discovered that the polarization of Rochelle salt ($NaKC_4H_4O_6*4H_2O$) reverses with the application of an external electric field. The phenomenon was first referred to as Seignette-electricity, in honor of the man who first developed Rochelle salt. However, the phenomenon was not studied extensively until simpler phosphates and arsenates, which exhibited the behavior, were developed in 1935-1938. [1] The term "ferroelectricity" came into common use in the early 1940s due to the easy analogies made between ferromagnetism and ferroelectricity.

Atoms in ferromagnetic materials have permanent magnetic dipoles. Unlike paramagnetic materials, the dipoles align spontaneously with each other. The source of this alignment is in the quantum mechanics of electrons in solids. The Curie temperature for a ferromagnetic material is the temperature at which the material becomes paramagnetic (ceases to be ferromagnetic). The Curie temperature for a ferroelectric is generally the point at which the material ceases to be ferroelectric.

Ferromagnetic domains are responsible for the hysteresis in the plot of magnetization vs. applied magnetic field. All of the dipole moments in a domain are aligned, and all of the dipole moments in neighboring domains are aligned in different directions. If the material is not magnetized, the sum of the fields due to all the domains is zero. When a field is applied, the domains line up parallel to that field. Magnetization saturates when the entire sample becomes one domain. When the field is removed, the domains do not go back to their original sizes, and a residual magnetization remains. Applying a magnetic field in the opposite direction can reverse the magnetization.

For a fresh (never polarized) ferroelectric crystal, the domains are aligned at random, resulting in zero net polarization. As an electric field is applied, the domains start to line up parallel to that field. At a sufficiently large field, all of the domains align to the field, indicating a state of saturation in which the crystal has become a single domain. Upon reversing the electric field, the polarization reverses but does not return to zero, the crystal has acquired a remnant polarization P_R. The remnant polarization can be removed by reversing the direction of the electric field to a coercivity value. This is the coercive field, E_C.

Ferroelectricity is quite a restrictive condition. Most materials are paraelectric, that is, polarization can be induced by an electric field, even though no permanent electric dipole exists. Ferroelectric crystals are polar. They contain a permanent electric dipole at the unit cell because of the local atomic arrangement. There are 32 crystal classes. Of these, 21 are non-centrosymmetric. Of these 21, 20 are piezoelectric: stress induces polarization. Only 10 of these piezoelectric classes are polar in the absence of stress. These 10 polar classes are pyroelectric: changes in temperature cause changes in polarization due to thermal expansion. Finally, if a crystal is polar, and the direction of polarization is switchable, then the crystal is ferroelectric.[2]

For many years, until quartz took over, ferroelectrics dominated in sonar detectors, phonograph pickups, and other piezoelectric applications. [1] Due to their pyroelectric properties, they can be used in infrared detection and imaging. The nonlinear electro-optic properties of ferroelectric materials make them of use in laser applications. None of these uses take advantage of the material's ferroelectric property, namely the large reversible spontaneous polarization which can be used in non-volatile memory applications. [3]

The focus of this thesis is the development of thin film ferroelectric devices, specifically, the deposition of ferroelectric lead zirconate titanate (PZT) by RF magnetron sputtering and by the chemical solution deposition (CSD) technique of spin-coating, and the integration of these films into ferroelectric capacitors which can be

used in memory applications. Development of a transparent ferroelectric capacitor and a transparent ferroelectric transistor is also explored.

The rest of this thesis is organized as follows. Chapter 2 provides a description of ferroelectric materials and devices including ferroelectric behavior of materials alone and in ferroelectric capacitors and transistors. Properties of different ferroelectric materials and processing issues are discussed with particular attention paid to lead zirconate titanate (PZT), the material used in the research for this thesis. Chapter 3 contains an explanation of the experimental technique used for this research, and descriptions of thin-film processing tool which were utilized. Chapter 4 presents procedure for fabricating PZT capacitors by RF magnetron sputtering and spin-coating as well as the results of electrical tests performed on them. Chapter 5 consists of a summary of the conclusions drawn from the experiments performed for this thesis and recommendations for future work on ferroelectric materials and devices.

2. LITERATURE REVIEW

The purpose of this chapter is to provide an overview of ferroelectric materials and devices, and the current state of technology for these materials and their applications. This chapter contains an explanation of the phenomenon of ferroelectricity. Ferroelectric materials physics is discussed and the specific case of ferroelectric perovskite crystals is explained. Common properties of the ferroelectric lead zirconate titanate are given. Material and device processing issues are discussed, specifically for ferroelectric capacitors and ferroelectric memory devices.

2.1 Ferroelectricity

The purpose of this section is to discuss the phenomenon of ferroelectricity, including the transition of a crystal to a ferroelectric phase, and the formation of domains and their role in the polarization of ferroelectric crystals. Finally, the specific case of the ferroelectric perovskite is discussed.

2.1.1 Ferroelectric phase transition

A ferroelectric phase transition is a structural phase transition which results in the ability of the crystal to sustain a spontaneous polarization, caused by the relative displacement of the ions of each unit cell of the crystal. [4]

The ferroelectric phase transition occurs at a temperature T_C, analogous to the Curie temperature of a ferromagnet. Above the Curie temperature, the crystal is usually a centrosymmetric paraelectric. Below the Curie temperature the crystal is no longer centrosymmetric, which results in ferroelectric behavior.

In the ferroelectric phase, at least one set of ions in the crystal sits in a double well potential, where either of two positions is equally energetically favorable. [3] Above T_C, the particles in the double well have enough kinetic energy to move back and forth over the barrier that separates the wells, so that the time average position

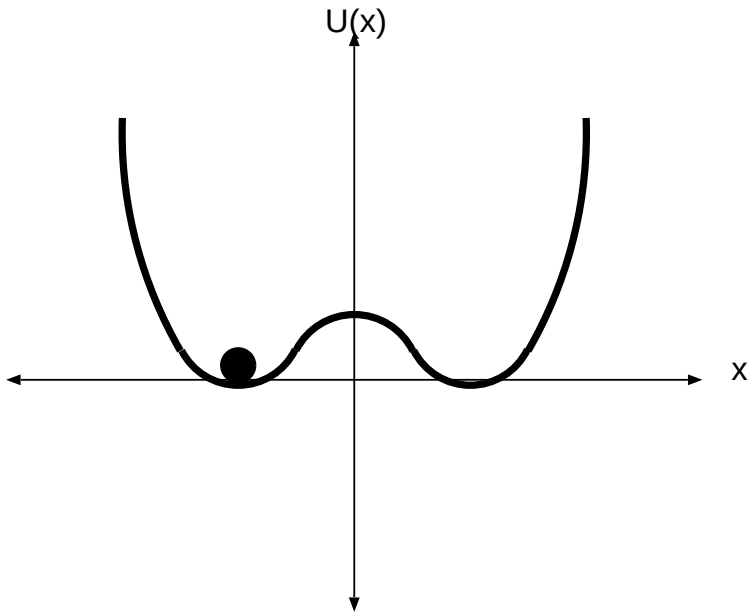

Figure 2.1: Thermodynamic potential as a function of atom position for a ferroelectric material below its Curie temperature. Conceptual atom sitting in one of two equally energetically favorable positions.

of the atom is midway between the wells. Figure 2.1 shows the thermodynamic potential of the system as a function of the atom position.

If the shape of the well stays the same above T_C, but the ion kinetic energy k_BT becomes large, the transition is an order-disorder phase transition. If the minima of the well actually move together to form a single well above T_C, then the transition is displacive. These are the extrema of the phase transition phenomena; most ferroelectric phase transitions are a combination of displacive and order-disorder transitions.

Ferroelectric phase transitions can be described mathematically with some success by Landau theory, often called Landau-Devonshire theory, as a credit to Devonshire, who developed it specifically for the ferroelectric case. Phase transitions in ferroelectrics are usually second-order transitions, meaning that the distortions of the crystal lattice occur continuously with temperature. When the transitions are discontinuous (first-order) they are usually close to second-order transitions and

are still described well by Landau-Devonshire theory. An exhaustive description of ferroelectric phase transitions can be found in reference [4].

In Landau-Devonshire theory, the Helmholtz free energy of the system is described by a power series in the order parameter. [3] For a ferroelectric crystal the order parameter is the polarization, η, where $0 \leq \eta \leq 1$,

$$F(\eta, T, E) = A\eta^2 + B\eta^4 + C\eta^6 + D, \tag{2.1}$$

where D is an inconsequential constant. A has the form $A_0(T - T_c)$, where T_c is the Curie temperature, which may not be equal to the transition temperature. If the transition is first-order, there is hysteresis in the temperature dependence. This form for A is a result of mean field theory, which is often used to describe ferromagnetism, but also works well for ferroelectrics. B and C are likely to be temperature dependent as well, but not strongly, so they are assumed not to be, for simplicity. The order (first or second) of the transition depends on the sign of B, with C being necessarily positive for stability. At thermal equilibrium, the free energy of any system is minimized,

$$\left(\frac{\partial F}{\partial \eta}\right)_{T,x} = 0, \tag{2.2}$$

$$0 = 2A\eta + 4B\eta^3 + 6C\eta^5. \tag{2.3}$$

If B is positive, the last term is negligible. Then

$$\eta^2 = 2A_0\frac{(T_C - T)}{4B}, \tag{2.4}$$

$$\eta(0)^2 = 2A_0\frac{(T_C)}{4B}, \tag{2.5}$$

$$\eta(T) = \eta(0)\sqrt{\frac{(T_C - T)}{T_C}}. \tag{2.6}$$

This describes the change in the order parameter as a function of temperature in the second-order, continuous phase transition. If B is negative, the transition is first-order, and discontinuous.

2.1.2 Domains and ferroelectric polarization

Ferroelectric behavior arises from the fact that in the ferroelectric phase, at least one set of ions in the crystal has a double-well potential as shown in Fig. 2.1. A local region where all of the ions in the crystal sit on the same side of the well is called a domain, analogous to domains in ferromagnetic materials. [3]

If a ferroelectric phase transition takes place in an ideal crystal with an infinitely slow decrease in temperature (to maintain thermal equilibrium throughout the crystal), then a single domain would form in the crystal. All ions in the crystal would be thermodynamically coupled and therefore sit on the same side of the double well, the probability of the ion residing in one side or the other being equal. In a real situation, different regions of the crystal which are sufficiently remote from one another form ferroelectric phases independently, resulting in domains with different directions of polarization.

In the equation,

$$\overline{D} = \epsilon_0 \overline{E} + \overline{P}, \tag{2.7}$$

which relates the electric displacement and electric field to the polarization, the dielectric polarization, $\overline{P}$, is due to both the polarizability of the material due to the applied field $\overline{P}_E = \chi \overline{E}$ and from the spontaneous alignment of dipoles in the material, $\overline{P}_S$.

The free charge density must satisfy Poisson's equation, $\nabla \cdot \overline{D} = \rho$ so that

$$\nabla \cdot \overline{E} = \frac{1}{\epsilon \epsilon_0}(\rho - \nabla \cdot \overline{P}_S). \tag{2.8}$$

In an infinite ideal ferroelectric crystal, $\nabla \cdot \overline{E} = \rho/\epsilon\epsilon_0$ as in ordinary dielectrics. For a real crystal, $\overline{P}_S$ goes to zero at the crystal surface, and may differ from the bulk crystal value at defect sites. For these reasons, $\nabla \cdot \overline{P}_S$ acts as a polarizing field opposed to the dielectric polarization. It is this depolarizing field which can be compensated by the flow of free charge in the crystal. The energy associated with the depolarization of the crystal is zero for a totally compensated crystal in equilibrium.

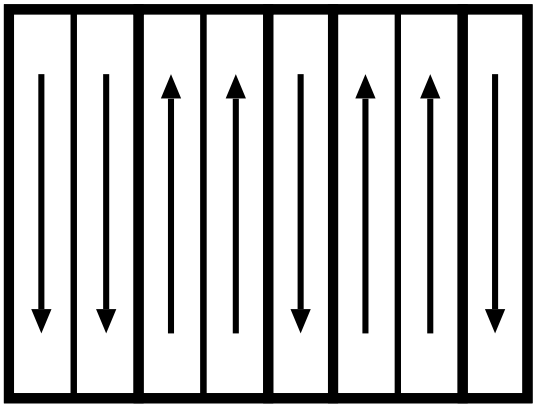

Figure 2.2: Columnar domain structure exhibiting random polarization.

[1] Domains form in fresh crystals to compensate for depolarization energy before free charge compensation takes place.

In a fresh crystal (one to which an electric field has never been applied) the net polarization of the crystal should be zero, due to the many domains of random polarization. In a nonconducting finite crystal, a complex, branched domain system is predicted to eliminate the electric field due to the surface. In real crystals, even a low conductivity can compensate the surface effects and allow for a simpler, columnar domain structure to form. [4] Figure 2.2 depicts a one-dimensional set of randomly aligned columnar domains which result in a zero net polarization of the crystal.

As in a ferromagnet, polarization of a ferroelectric crystal is accomplished by aligning all of the cells in the material in the same direction, by the application of a field. This is accomplished by increasing the size of domains in the desired direction, while decreasing the size of domains in the other direction, until the crystal is one domain pointing in the direction of the applied field.

Domain walls in ferroelectrics are only a few unit cells wide, with the polarization going to zero at the center of the wall. The domain width is dependent on the thickness of the crystal. If the thickness of the crystal decreases so that the domain width approaches the thickness of the domain wall, the depolarizing field can no longer

be compensated, and there is believed to be a minimum film thickness for which ferroelectricity is a stable state. [1] The occurrence of a finite thickness has considerable implications for applications of ferroelectrics, because it limits the useful thickness of these materials. Theoretical attempts to determine the minimum thickness for $Pb(Zr,Ti)O_3$ found it to be about 20 nm at room temperature. [5] Calculations for stress-free nonconducting $Pb(Zr,Ti)O_3$ films find that ferroelectricity could be stable down to a monolayer. [6] These circumstances are extremely unlikely to occur, but atomically smooth films down to 4 nm have exhibited ferroelectric polarization. [5]

The primary property of a ferroelectric is the reversibility of its spontaneous polarization, accomplished by reversing the direction of the applied field. Polarization is demonstrated by a hysteresis loop in the plot of polarization (charge per unit area) versus applied electric field (P-E). This is measured using a modified Sawyer-Tower circuit. [7]

Figure 2.3 illustrates the important features of a P-E plot. The coercive field, E_C, is the field at which half of the polarization has been reversed. The remnant polarization, P_R, is the polarization which remains when the field returns to a zero value. A high polarization and a low, well-defined coercive field result is a square-shaped hysteresis loop and crystal properties that are favorable for ferroelectric device applications.

Defects in ferroelectric crystals are evident in the P-E plot. When the polarization is reversed, the polarization due to defects may not reverse, or may reverse at a different field than the rest of the crystal. If the defects do reverse, this affects the value of the coercive field. If the defects do not reverse, the whole loop is biased along the field axis.

The hysteresis loop observed using the Sawyer-Tower circuit is a vital tool in characterizing ferroelectric crystals and is be discussed further in Chapter 3 of this thesis.

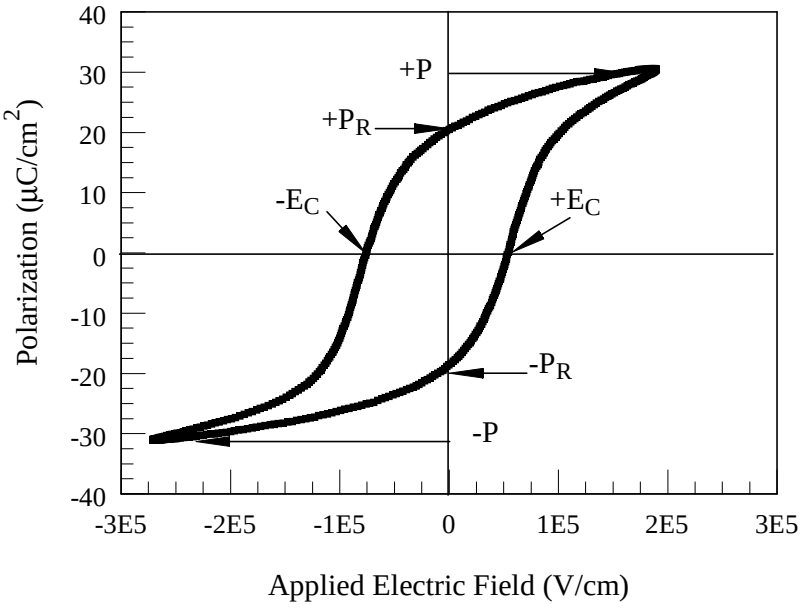

Figure 2.3: Typical hysteresis loop for a ferroelectric material. Coercive field and polarization values are indicated.

2.1.3 Perovskite crystals

Perovskite-type ferroelectrics have been extensively studied due in large part to the simplicity of the perovskite structure, and the relatively common occurrence of ferroelectric behavior in perovskites.

A perfect perovskite crystal is cubic, with the general formula ABO_3. The A atoms on the crystal corners are monovalent or divalent metal. The B atom is at the body center and is a tetravalent or pentavalent metal. The oxygen atoms are at the face centers of the cube. [1] The cubic shape, as shown in Fig. 2.4 (a), is the prototype shape of the perovskite, and is the shape of the paraelectric phase. Below the Curie temperature, the cubic lattice is tetragonally distorted (Fig. 2.4 (b) and (c)), which is a displacive ferroelectric phase transition. Some materials also exhibit a rhombohedral ferroelectric phase. [1]

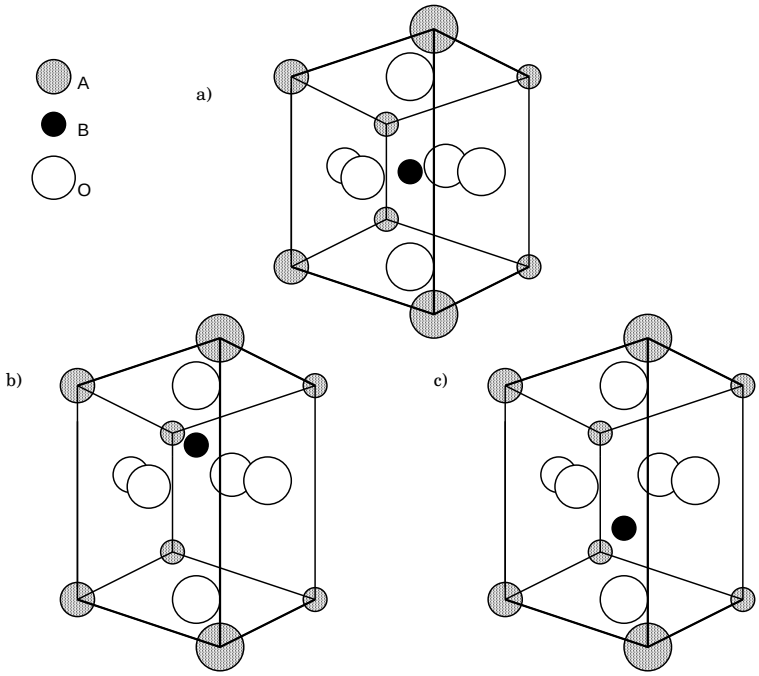

Figure 2.4: Cubic (a) and tetragonally distorted perovskite crystal cells with up (b) and down (c) polarized B atoms.

It is the off-centering of the B cation that leads to ferroelectric and antiferroelectric behavior. The B cations have two stable positions relative to the neighboring ions. A potential barrier separates one position from the other. The ion can change positions if enough energy is supplied to the system to allow the ion to surmount the barrier. For a single cell of lead zirconate titanate, this is less than thermal energy at room temperature, so the ion is free to move back and forth. In a crystal, however, the cells couple electrically and physically to form domains, as discussed in Section 2.1.2, for which the energy barrier to switching is much higher than for the single cell. [8]

2.2 Lead zirconate titanate

Lead zirconate titanate (PZT) is a solid solution of the perovskites lead zirconate and lead titanate. This section contains a description of lead titanate and

lead zirconate and the effects of mixing them in varying composition. Material defects are discussed, as well as the methods to prevent or circumvent defect-related problems. Finally, PZT is compared to other common ferroelectric perovskites.

2.2.1 Lead zirconate and lead titanate

Lead titanate ($PbTiO_3$) is a commonly studied ferroelectric material. It seems to be a textbook example of a ferroelectric phase transition [1] and it crystallizes in the perovskite phase, showing good polarization characteristics, at low process temperatures (less than 500 °C). [9] $PbTiO_3$ has a band gap of 3.4 eV and an electron affinity of 3.5 eV. [10] Leakage current due to electron injection from the electrode occurs when low work-function materials are used as electrodes. This phenomenon is discussed further in Section 2.3.1.

Lead zirconate ($PbZrO_3$) is a perovskite which shows characteristic antiferroelectric behavior. In an antiferroelectric crystal, neighboring lines of ions displace in opposite directions, creating a zero net polarization that is different from the zero net polarization caused by the random alignment of ions in an unpolarized ferroelectric crystal. [11] At high applied fields, antiferroelectric crystals behave like ferroelectric crystals.

$PbZrO_3$ has a band gap 0.3 eV larger than $PbTiO_3$ and an electron affinity 0.3 eV smaller. [10] These properties make $PbZrO_3$ attractive for improving transparency and minimizing leakage when it is combined with $PbTiO_3$

The solid solution $Pb(Zr_x,Ti_{1-x})O_3$, called PZT, is best known for its exceptional piezoelectric properties. Compositions with different values of x have been studied for applications in ferroelectric devices. At very high values of the Zr/Ti ratio (95/5) the material behaves like an antiferroelectric, exhibiting a double hysteresis loop when the material switches from antiferroelectric to ferroelectric due to the applied field. [12]

Films with lower Zr/Ti ratios tend to have lower crystallization temperatures [13], but films with higher Zr/Ti ratios have lower coercive fields, higher remnant polarization, and higher optical transmittance. [14]

2.2.2 Material process issues for PZT films

In order to use ferroelectric films in devices, the film quality must be optimized. A good ferroelectric film has a high remnant polarization (a large amount of charge can be stored in a small area), and a small coercive field (can be polarized at low voltages). A well-defined coercive field is also desirable and is evident from a more square-shaped hysteresis loop. For use in transparent devices, a high optical transmittance for visible light is also required.

Most defects in PZT are due to vacancies, usually lead and oxygen. PbO is volatile and PZT can accommodate large amounts of lead and oxygen vacancies which can interact with one another. [15] Low resistivity is also attributed to lead loss in PZT films. Lead loss is avoided by adding 10% or more excess lead to spin solutions or sputter targets [16, 17, 18]. Oxygen vacancy formation is inhibited by including donor dopants in PZT.

Lead loss causes PZT to behave like a p-type semiconductor. The lead vacancies (V_{Pb}) act as acceptors and cause the Fermi level to move toward the valence band. [19] When it is thermodynamically more favorable to create an oxygen vacancy (V_O) to compensate the lead vacancy than it is to further modulate the Fermi level, oxygen vacancies form concomitantly with lead vacancies, and the material exhibits fatigue and conductivity. Figure 2.5 shows the relationship between the oxygen and lead vacancies and the Fermi level in the PZT band gap.

The migration of oxygen vacancies during polarization causes fatigue. [20] Intentional donor doping has been shown to counteract fatigue in ferroelectric capacitors, presumable by the suppression of the formation of oxygen vacancies. Fatigue occurs when, upon repeated switching of a crystal, the polarization becomes clamped

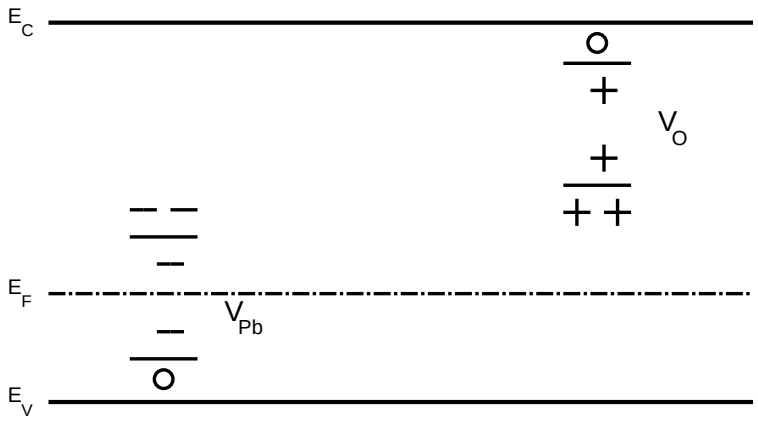

Figure 2.5: Lead and oxygen vacancies in the PZT band gap, leading to p-type conductivity. The lead vacancy is a double acceptor and the oxygen vacancy is a double donor, as indicated.

while the coercive field increases and becomes less well defined. Fatigue causes a longer switching time for the crystal. [1] Besides donor doping, fatigue can be reduced or eliminated by choosing oxide electrodes. This is discussed in more detail in Section 2.3.1.

It is common practice to include donor dopants in PZT, to improve electrical and optical properties. The most common A-site dopants are trivalent lanthanum (La) and yttrium (Y). Lanthanum donor dopants in PZT compensate the lead vacancy acceptors, threby inhibiting the formation of oxygen vacancies. Figure 2.6 shows La donor sites in the band gap. (Pb,La)(Zr,Ti)O_3, PLZT is valued for its exceptional electro-optic properties, and its increased transparency compared to PZT. [14, 18] However, PLZT has a smaller amount of polarization and a less square hysteresis loop when compared to PZT with the same Zr/Ti ratio. [15]

Common B-site donor dopants are pentavalent niobium (Nb) and tantalum (Ta), which substitute for quadrivalent Zr or Ti. Niobium-doped PZT exhibits an increase in crystal grain size, but also the introduction of a non-ferroelectric pyrochlore

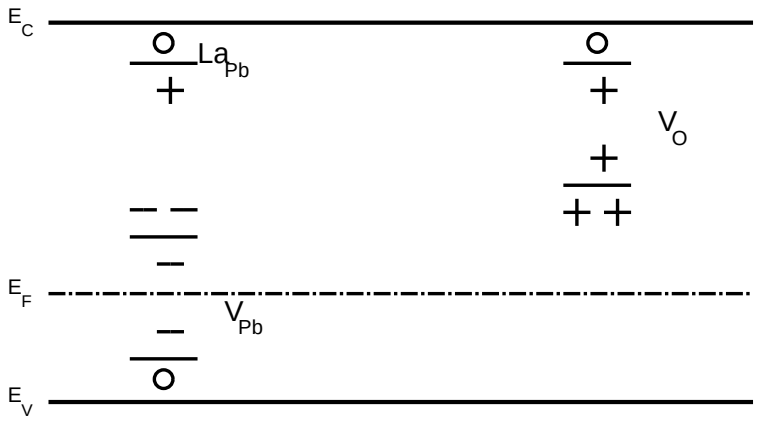

Figure 2.6: Lanthanum donors in the band gap of PZT compensate lead vacancies, leading to the suppression of compensation-induced oxygen vacancies.

phase, $Pb(Zr,Ti)_2O_7$, at Nb concentrations greater than 4 percent for spin-coated films. [15]

The introduction of a pyrochlore phase, which results in a lower polarization, can be a problem in undoped PZT and PLZT as well as Nb-doped PZT. A thin layer of $PbTiO_3$ deposited before PZT or PLZT has been shown to assist in the crystallization in the perovskite phase [17, 21] since $PbTiO_3$ always crystallizes in the perovskite phase. Very thin $PbTiO_3$ layers have worked well to facilitate growth of the perovskite phase and have little effect on the dielectric properties of the film, but increasing the thickness of the $PbTiO_3$ buffer layer causes a decrease in the dielectric constant due to the lower dielectric constant of $PbTiO_3$ versus PZT. [21]

Other methods of crystallizing films in the perovskite phase are to heat the substrate during deposition, or post-deposition annealing of the film. Thomas *et al.* [16] used a combination of substrate heating and post-deposition annealing to obtain a single phase perovskite film by RF sputtering. Yamakawa *et al.* [22] achieved a perovskite phase of PZT using successive millisecond cycles with a flash lamp at 27 J/cm^2.

2.2.3 Other Perovskite Ferroelectrics

The discovery of the first ferroelectric perovskite, barium titanate, $BaTiO_3$, led to an enormous rise in interest in ferroelectrics in the 1950's. [1] Although PZT is by far the most commonly studied and used ferroelectric material today, due to its large remnant polarization and piezoelectric properties, the leakage and fatigue problems associated with PZT, its tendency to interdiffuse with silicon, and the toxicity of lead has prompted researchers to search for other viable ferroelectric materials. The perovskite structure is so often ferroelectric, that it is not surprising that other ferroelectric perovskites have been found with desirable properties for silicon microstructure processing.

The band gap of $BaTiO_3$ (BTO) is 3.3 eV, large enough to make it transparent, and the electron affinity is 3.9 eV, which may make leakage current due to Schottky emission a problem. [10] It also has a relatively low Curie temperature of 135^oC [1]. $SrTiO_3$ has a Curie temperature below freezing, making it impossible to use as a ferroelectric at room temperature, although it has been used as a buffer layer to grow other perovskite films and as a diffusion barrier. [23]

The compound $Ba_xSr_{1-x}TiO_3$ (BST) does not have as high a dielectric constant or remnant polarization as PZT, but it does have lower leakage properties. BST can be deposited by chemical solution deposition (CSD) and metal organic chemical vapor deposition (MOCVD) [24]. It has a relative dielectric constant of about 260 in thin films. The dielectric behavior of BST is nonlinearly dependent on the thickness of the film. [25]

A likely replacement for PZT in ferroelectric applications is $SrBi_2Ta_2O_9$ (SBT). SBT is a layered perovskite consisting of two layers of perovskite $SrTaO_3$ followed by a layer of BiO_2. It has a wide band gap (4.1 eV), a small electron affinity (3.5 eV) [10], a high Curie temperature (335 °C) [1], and a high dielectric constant (up to 500). It seems to be a good choice for many ferroelectric applications, but high processing temperatures (750 - 800 °C) have made integration with other devices difficult. [25]

Efforts to lower the processing temperature of SBT have yielded good films at about 600 °C, which is still too high for many applications. The Bi in SBT is volatile and can be deficient in as-grown films if the process is not tightly controlled. [24] Bi also has a tendency to diffuse into top and bottom Pt electrodes, prompting study of barrier layers. [26] SBT can be deposited by CSD methods, and it does not suffer from fatigue or leakage to the extent that PZT can. It has a lower coercive field, but also a lower remnant polarization than PZT. [27, 28] SBT can be deposited onto Si without significant interdiffusion at the SBT/Si interface [29].

2.3 Ferroelectric capacitor memory devices

The inherent memory derived from the spontaneous polarization of ferroelectric materials has already been used in ferroelectric memories based on the Dynamic Random Access Memory (DRAM) one transistor/one capacitor (1T/1C) design. This section contains a discussion of the device process issues involved in fabricating ferroelectric capacitors, a description of the operation of a 1T/1C RAM device, and the operation of a ferroelectric RAM (FRAM) device.

2.3.1 Ferroelectric capacitors

One way that the study of ferroelectric materials is more complicated than the study of ferromagnetic materials is that in order to apply a polarizing field to a ferroelectric, one must make electrical contact to the ferroelectric material, which is not necessary when applying a magnetic field to a ferromagnetic material. The simplest structure with which to study ferroelectric behavior is a capacitor. A metal-ferroelectric-metal (MFM) structure is one in which the metal, or conducting metal oxide, is applied directly to the ferroelectric material. A desirable structure for the semiconductor industry is an MFS structure, a variation of the metal-oxide-semiconductor (MOS) structure. Processing incompatibilities have turned this into

an MFIS structure, where one or more additional insulators are inserted between the semiconductor and the ferroelectric.

A good capacitor for use in commercial devices has low leakage, good resistance to breakdown, and uniform properties. The choice of electrode material is imperative to the reliability of ferroelectric capacitors. An electrode must have low resistance, adhere to the ferroelectric and the layers under the electrode, and provide a chemically stable environment for growth of the ferroelectric material and operation of the device. The bottom electrode can aid or inhibit PZT growth in the perovskite phase.

Imprint is a problem in ferroelectric capacitors that is almost always associated with oxygen vacancies. Imprint is characterized by a horizontal shift of the hysteresis loop of the P-E plot due to the development of an internal electric field. The field is caused by the movement of ionic defects such as oxygen vacancies.

Fatigue is often seen in ferroelectric capacitors. It is characterized by a decrease in switching polarization with repeated cycling. Fatigue has been attributed to electronic pinning and unpinning of domain walls during polarization reversal, and to ionic defects, more specifically, oxygen vacancies. The fact that fatigue effects are reduced when oxide rather than metal electrodes are used supports both mechanisms as the cause of fatigue. Metal electrodes form a Schottky barrier with the ferroelectric, and electrons at the interface are suggested as interacting with and pinning the domains at the surface, and thus reducing the switching polarization. [15]

Lead-site donor doping has been used to reduce fatigue in PZT, as discussed in Section 2.2.2. Doping with lanthanum decreases the remnant polarization of the device, so Myers [20] made a capacitor using thin layers of PLZT at the electrodes, with a PZT layer in the middle. This results in a device that, although more complicated to process, optimizes the use of the properties of both the doped and undoped film.

Another way to avoid fatigue in ferroelectric capacitors is to use an oxide electrode. The use of oxide electrodes has been shown to eliminate polarization fatigue. Oxide electrodes act as sinks for oxygen vacancies. [15]

Conducting oxides with a rutile-type crystal structure have been proposed as electrodes for PZT. Experiments using RuO_2 have shown improved fatigue properties, but increased leakage, believed to be due to a conductive Pb_2RuO_{7-x} layer at the interface [30]. PZT does not grow phase-pure on RuO_2. IrO_2 is another rutile-type conducting oxide used as a PZT electrode. Problems associated with fatigue are reduced when an IrO_2 electrode is used, despite the interdiffusion of Ir with PZT. [15]

$La_{0.5}Sr_{0.5}CoO$ (LSCO) is a conducting oxide which is itself a perovskite material, which makes it ideal for growth of perovskite PZT. LSCO electrodes improve fatigue effects and a fully oxygenated LSCO electrode capacitor exhibits no imprint. [15] [27] The work function of LSCO is 4.65 eV [31], providing a Schottky barrier height of 1.15 eV and low leakage current. LSCO can stand high temperature processing (600 - 800 °C) and processing in an oxygen ambient improves its conductivity, making it favorable for use in PZT processing when transparency is not important. LSCO and $LaNi_{0.6}Co_{0.4}O_3$ (LNCO), both perovskites, have been shown to reduce fatigue phenomena even when the oxide electrode is used only on one side of the ferroelectric PZT layer. [32]

As a transparent electrode, ITO seems an appropriate choice. [33] The Schottky barrier height for ITO on PZT is small enough to make leakage current a possible problem, but the ITO/PZT interface shows very little interdiffusion under TEM observation. [34] Table 2.3.1 lists possible electrodes to PZT and the resulting Schottky barrier heights.

Noble metals such as Pt, Au, Ir, and Ni form Schottky contacts with PZT. Dawber *et al.* [38] found that breakdown in PZT capacitors is dependent on the work function of the cathode material, indicating that electrons are injected into the

Table 2.1: Work functions of common contact materials to PZT and their expected Schottky barrier heights to $PbTiO_3$ (electron affinity = 3.5 eV, from [10]), using ideal Schottky barrier theory in which the barrier height is estimated as the metal work function minus the semiconductor electron affinity.

Material	Work Function	Schottky Barrier Height to $PbTiO_3$ (eV)	Transparent	Reference
Au	5.1	1.6	No	[35]
Ni	5.2	1.7	No	[35]
Pt	5.6	1.1	No	[35]
Al	4.3	0.8	No	[35]
Ir	5.3	4.8	No	[35]
LSCO	4.65	1.15	No	[31]
In_2O_3	3.7	0.2	Yes	[36]
SnO_2	4.6	1.1	Yes	[37]

ferroelectric. Schottky barrier electrodes limit the leakage current, and the leakage current is higher with rutile oxide electrodes than with Pt electrodes. [31] Figure 2.7 depicts the energy band diagram when ITO and Au are used as electrodes to PZT.

The MFIS structure has been proposed as another solution to fatigue problems as well as interface (diffusion) problems and leakage current. Kim *et al.* [39] attempted to use this structure with SBT. Their capacitors no longer saturate at reasonable voltage for semiconductor microchip applications. They do demonstrate hysteresis in the C-V curve.

The reason that it is difficult to saturate the MFIS structure is the vast difference in dielectric constant between the ferroelectric and the insulator layers. The addition of insulating layers to a ferroelectric capacitor may help with the challenge of integrating PZT onto silicon wafers.

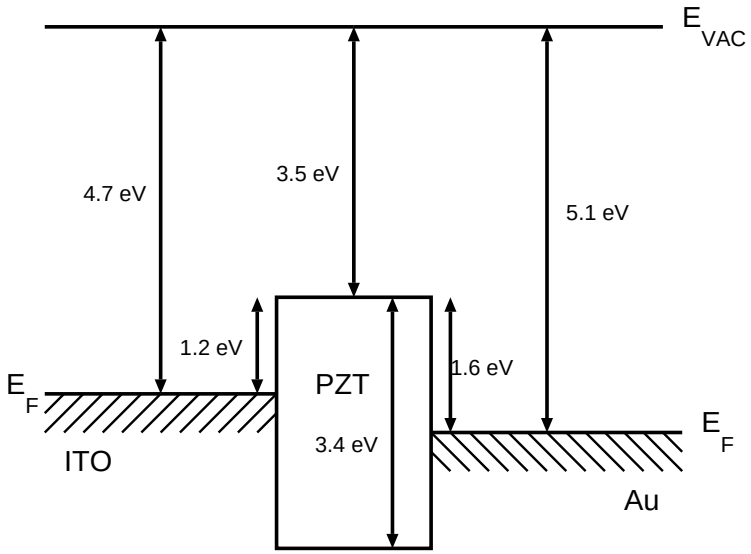

Figure 2.7: Energy band diagram of a ferroelectric capacitor with ITO and Au contacts. Electron affinity and Schottky barrier information are indicated.

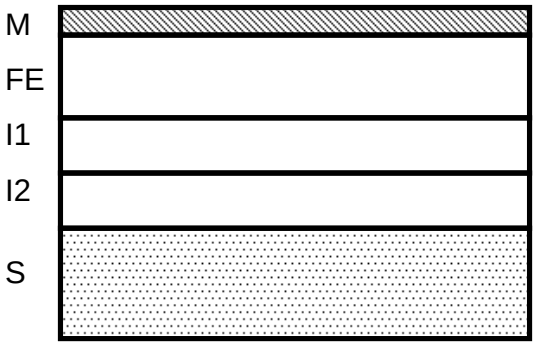

Figure 2.8: Metal ferroelectric insulator semiconductor (MFIS) capacitor structure.

In the simplest case, the MFIS structure is a series of capacitors, each with capacitance $C = \epsilon A/d$, dependent on the dielectric constant ϵ and the thickness d of the respective dielectric layer. All have the same area, A defined by the area of the contacts. The total effective capacitance per unit area of the stack is given by

$$C_{EFF} = [(C_{FE})^{-1} + (C_{I1})^{-1} + (C_{I2})^{-1}]^{-1}, \tag{2.9}$$

$$C_{EFF} = [\frac{d_{FE}}{\epsilon_{FE}} + \frac{d_{I1}}{\epsilon_{I1}} + \frac{d_{I2}}{\epsilon_{I2}}]^{-1}. \tag{2.10}$$

I2 is usually SiO_2, which has a relative dielectric constant of 3.9, and I1 is a high dielectric constant buffer layer to prevent Si-Pb interdiffusion. Assume it has a relative dielectric constant of 20. If the the ferroelectric is PZT and the dielectric layers are of comparable thickness

$$\frac{1}{C} = \frac{V}{Q} = \frac{1}{500} + \frac{1}{20} + \frac{1}{3.9}. \tag{2.11}$$

Therefore, only 1/500 of the voltage applied to the stack actually drops on the ferroelectric layer. In order to have the same voltage drop on all three layers, set

$$\frac{d_{FE}}{\epsilon_{FE}} = \frac{d_{I1}}{\epsilon_{I1}} = \frac{d_{I2}}{\epsilon_{I2}}. \tag{2.12}$$

The thickness of the I2 layer is the native oxide thickness of SiO_2, which is 1 nm. This determines the thickness of the buffer layer to be 5.12 nm and the ferroelectric layer to be 128 nm. In this case, only 1 of every 3 volts applied to the stack drops across the ferroelectric layer. If it usually takes 5 V to polarize a 128 nm thick ferroelectric layer, 15 V must be applied to the MFIS device. To increase the voltage drop on the ferroelectric, the ferroelectric layer must be made thicker.

An MFIS device will require more voltage to operate than an MFM device with the same ferroelectric layer thickness. Or, the ferroelectric layer in the MFIS device will have to be 10 or 100 times thicker than the MFM capacitor.

The voltage drop on the non-ferroelectric insulator(s) of the MFIS device can also have implications on the performance of memory devices based on the MFIS capacitor, so this device is discussed further as appropriate in the following sections.

2.3.2 RAM-type ferroelectric memory

The reversible spontaneous polarization of ferroelectric materials make them attractive for memory applications. And ideal memory device has low power consumption, fast read and write access times, and infinite rewritability. Memory devices should also be scalable, so that they can be made smaller as size requirements change. A ferroelectric non-volatile (NV) memory must be able to maintain its orientation in the absence of applied power for more than ten years in order to compete with modern devices. [40]

Designs for ferroelectric memory have two basic types; capacitor-type memories have a ferroelectric capacitor in series with a field-effect transistor (FRAM), and transistor-type memories have a ferroelectric material in the gate dielectric (FEFET).[28] FEFETs are discussed in Section 2.4.

Non-volatile ferroelectric random access memory (NVFRAM) are the first ferroelectric devices to be commercially available. [41]

Memory arrays of capacitor-type FRAM have advantages over current magnetic hard disks and floppy disks in that they have no moving parts, are more reliable, and have faster read/write access times. Also, ferroelectric materials have dielectric constants up to 500 times larger than current memory dielectrics, so more charge can be stored in a smaller surface area. [40]

FRAM is based on the DRAM structure in which a capacitor is connected in series with a transistor. Figure 2.9 depicts a circuit diagram of a FRAM device. The success of DRAM is due largely to its small cell size. DRAM and FRAM store one bit on one capacitor and one transistor. [42]

Data are stored in an array of capacitors, each connected to the source of a MOS transistor. The drains of the transistors are connected to the bit lines, and the gates are connected to the word lines. Data are written to the capacitors by applying a voltage to the word line to turn on the transistors, which has the effect of connecting each capacitor to its bit line. Then a voltage greater than the ferroelectric capacitor's

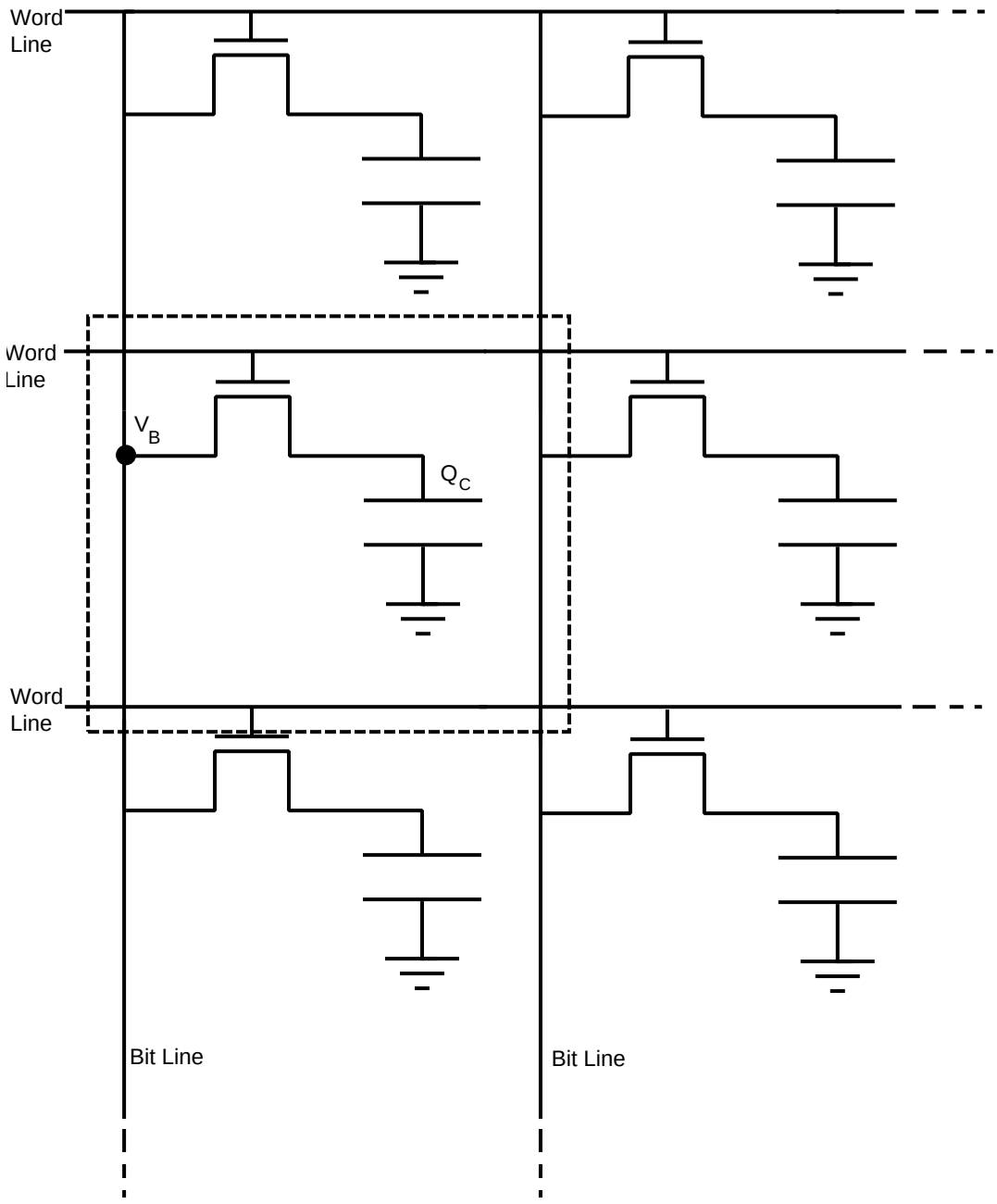

Figure 2.9: FRAM circuit diagram with one memory cell indicated.

positive coercive voltage or a voltage greater than the capacitor's negative coercive voltage is applied to the bit line to write 1 or 0 to the cell, respectively.

To read the cell, the transistors are turned on, and the capacitors discharge onto the bit line. At the end of each bit line, a sense amplifier determines whether the cell was written with a 1 or a 0, and then rewrites the cell by applying the appropriate voltage. DRAM is volatile, the capacitors must be refreshed occasionally to maintain the memory (charge).

The advantage of using a ferroelectric capacitor in a DRAM cell is the non-volatility of the ferroelectric polarization. An FRAM, ideally, is a NV memory that is as small as a DRAM cell, with no moving parts. Also, as feature size shrinks, it has become more and more difficult for device engineers to find a way to store the requisite charge in a smaller area. Trench and stacked capacitors have worked in the past, but cell height is becoming an issue. Trenches cannot be made deeper with current lithography techniques. This is a situation in which the high dielectric constant of ferroelectric materials is again useful. When a material has a higher dielectric constant, more charge can be stored in a smaller area.

Like DRAM, FRAM is a destructive read-out (DRO) device, which means that the information stored in the cell is lost when the cell is read, and must be rewritten after it is read. Reading an FRAM cell requires that the polarization on the capacitor be reversed. This means that FRAM devices will be read and rewritten more often than nondestructive read-out (NDRO) devices. The quality of the capacitor is integral to the device properties. Fatigue in ferroelectric capacitors is a serious problem in DRO devices, since fatigue is a loss of ferroelectric properties with increased cycles of polarization. For the capacitor to be read and written again and again and maintain the on-off ratio of the device, the capacitor must not exhibit fatigue. [25, 43]

It is also important that the devices be symmetric, that is, the positive and negative coercive voltages have approximately the same value, which remains constant in time. Since the device is written with a 1 or a 0 with a voltage pulse that is greater

than the coercive voltage, the coercive voltage must remain the same over time in order to properly polarize the device with that pulse. For this reason, only capacitors which exhibit good fatigue and imprint properties can be used in FRAM devices. The migration of the coercive field that is accompanied by imprint can cause the device to not polarize or depolarize completely, leading to device failure. The two coercive voltage points should be symmetrical and less than 2.5 V in order to operate from standard memory power-supply voltages. [40]

Ferroelectric capacitors are usually integrated onto a CMOS processed chip in a back-end process to keep from contaminating the CMOS facility. This means that all of the processes involved in depositing and patterning the ferroelectric capacitors have to be safe for the CMOS devices [41], and must not damage the ferroelectric layer. [28]

2.4 Ferroelectric transistor memory devices

Transistor-type memories have a much smaller cell area, since the memory element is in the gate electrode. They are non-destructive read-out (NDRO) devices, and non-volatility is a challenge that transistor memories have yet to overcome.

FEFETs are usually field-effect transistors with a MFS or MFIS capacitor as a gate control. Memory retention times of a few hours are common, with the best devices having a retention time of a few days. The challenge of memory retention and good switching performance has prompted many variations on the FEFET device.

Most FEFETs are MFISFETs. A buffer insulator layer between the ferroelectric material and the Si layer is used as a diffusion barrier between PZT and Si, to prevent current leakage through the gate. The two main problems facing the MFISFET, as discussed by Ma *et al.* [44] are a low on/off ratio caused by a depolarization field, and gate leakage, which causes a loss of polarization over time.

The spontaneous alignment of dipoles in a ferroelectric gives rise to a depolarization field which is proportional to the charge (per unit area) on the surfaces of the

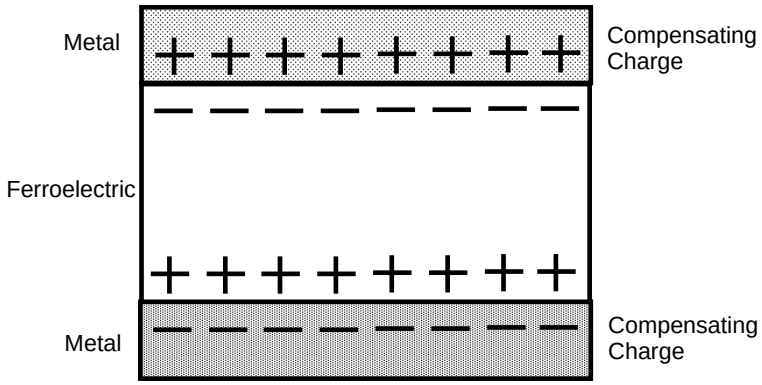

Figure 2.10: MFM structure with charge-compensating electrodes.

ferroelectric material. [45] The magnitude of the depolarization field is given by

$$E_{DEPOL} = \frac{P}{\epsilon_{FE}\epsilon_0} \tag{2.13}$$

In an MFM structure such as the one shown in Fig. 2.10, the polarization charge at the ferroelectric surface attracts opposite charge from the metal, and this compensating charge eliminates the depolarization field. The lower carrier density in semiconductors (and very low carrier density in insulators) results in insufficient charge close to the ferroelectric surface, and a residual depolarization field exists.

Consider the MFIS structure shown in Fig. 2.8. The insulator and semiconductor layers can be grouped together. From Kirchhoff's voltage law, the total voltage dropped across the device is the sum of the voltage drops across each layer, or,

$$V = V_{FE} + V_{IS}. \tag{2.14}$$

From Kirchhoff's current law, the charge on the ferroelectric layer is equal to the charge on the insulating layer,

$$Q_{FE} = Q_{IS}. \tag{2.15}$$

The boundary conditions for the structure are

$$Q_{IS} = \frac{\epsilon_{IS} V_{IS}}{d_{IS}}, \tag{2.16}$$

and

$$Q_{FE} - P = \frac{\epsilon_{FE} V_{FE}}{d_{FE}}. \tag{2.17}$$

An applied voltage, V, causes polarization, P, in the ferroelectric. First, solve Eq. 2.14 for the voltage across the ferroelectric,

$$V_{FE} = V - V_{IS}. \tag{2.18}$$

Since $C = \epsilon/d$ (per unit area), Eq. 2.16 can be written

$$V_{IS} = \frac{Q_{FE}}{C_{IS}}, \tag{2.19}$$

where Eq. 2.15 was used to substitute Q_{FE} for QIS. Using the capacitance equation again to rearrange Eq. 2.17 gives

$$Q_{FE} = C_{FE} V_{FE} + P. \tag{2.20}$$

Using this equation in Eq. 2.19 and using the resulting equation for V_{IS} in Eq. 2.18 give the following expression for V_{FE},

$$V_{FE} = \frac{C_{IS} V}{C_{IS} + C_{FE}} - \frac{P}{C_{IS} + C_{FE}}. \tag{2.21}$$

Next, include the magnitude of the depolarization field as expressed in Eq. 2.13,

$$V_{FE} = \frac{C_{IS} V}{C_{IS} + C_{FE}} - \frac{E_{DEPOL} \epsilon_{FE} \epsilon_0}{C_{IS} + C_{FE}}. \tag{2.22}$$

The dielectric constants and thicknesses of the ferroelectric and insulating layers can be substituted into Eq. 2.22 to show more explicitly the affect of these parameters,

$$V_{FE} = \frac{\frac{\epsilon_{IS}}{d_{IS}} V}{\frac{\epsilon_{IS}}{d_{IS}} + \frac{\epsilon_{FE}}{d_{FE}}} - \frac{E_{DEPOL} \epsilon_{FE}}{\frac{\epsilon_{IS}}{d_{IS}} + \frac{\epsilon_{FE}}{d_{FE}}}. \tag{2.23}$$

Simplifying Eq. 2.22 gives

$$V_{FE} = \frac{V}{1 + \frac{\epsilon_{FE}}{\epsilon_{IS}} \frac{d_{IS}}{d_{FE}}} - \frac{E_{DEPOL}}{\frac{\epsilon_{IS}}{\epsilon_{FE} d_{IS}} + \frac{1}{d_{FE}}}. \tag{2.24}$$

In Eq. 2.24, if the thickness of the insulating layers, d_{IS}, goes to zero, $V_{FE} = V$, and all of the applied voltage is dropped across the ferroelectric, and no depolarization

field exists. If ϵ_{IS} goes to infinity, which is the case of a metal contact, the depolarization field again is reduced to zero. The strength of the depolarization field can be controlled by controlling the thickness and dielectric constant of the insulating and semiconducting layers. It can be reduced by using a higher dielectric constant ferroelectric layer, and a high dielectric constant and very thin insulator layer, and by using a very thin semiconductor layer channel layer.

The static depolarization field is opposed to the direction of ferroelectric polarization and reduces the on/off ratio of these devices. As long as C_{IS} is finite, a depolarization field always exists.

Ferroelectric transistor memories are written by applying a gate voltage to the device, usually a pulse long enough to polarize the ferroelectric. When the ferroelectric layer has been polarized, a channel is induced or depleted in the semiconducting layer. The device is read by examining the source-drain current. For a device which has been written in such a way that the channel is depleted, the source-drain current is very small. Figures 2.11 and 2.12 illustrates the manner in which a depolarization field can reduce the on/off ratio of a FEFET memory.

First consider the MFM structure whose energy bands are illustrated in Fig. 2.11. When no voltage has been applied, the ferroelectric is unpolarized and a flat band situation exists (Fig. 2.11 (a)). To polarize the ferroelectric, a voltage V is applied which is greater than the coercive voltage for the device (Fig. 2.11 (b)). When the applied voltage is removed, the ferroelectric remains polarized (Fig. 2.11(c)). The polarization is the remnant polarization of the ferroelectric which results in a voltage V_R on the device which is less than the formerly applied voltage.

Next, examine the energy band diagrams for the MFIS structure, which are indicated in Fig. 2.12. Figure 2.12 (a) shows the flat-band case for an MFIS device with a p-type semiconductor. In order to program this device into its "on" state, a negative gate voltage is applied to polarize the ferroelectric in order to induce and inversion layer in the p-type semiconductor. During the write pulse, a negative

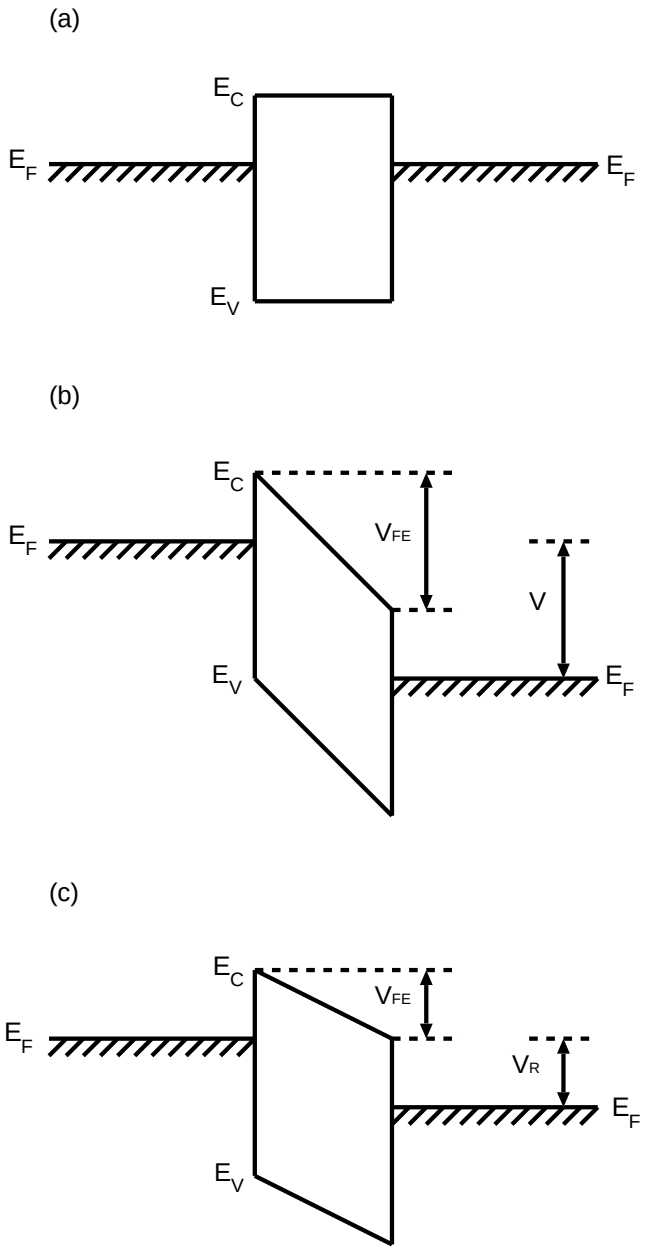

Figure 2.11: Energy band diagram of an MFM capacitor. (a) Flat band. (b) During polarization voltage pulse. (c) After pulse is removed, remnant polarization results in a persistent remnant voltage, V_R.

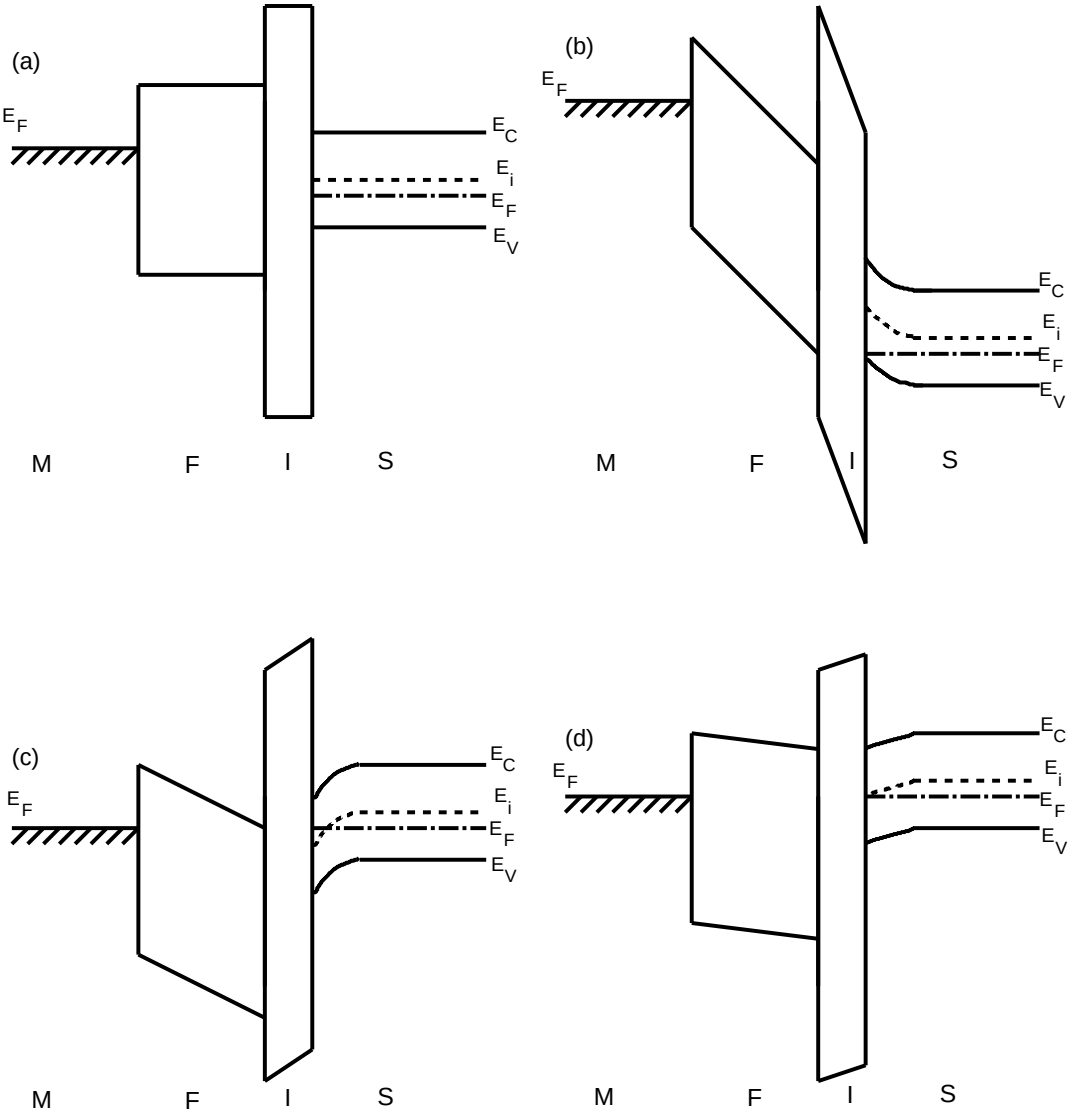

Figure 2.12: Energy band diagram of an MFIS capacitor which would be used as a gate control for a FEFET memory transistor. (a) Flat band. (b) During polarization voltage pulse. Semiconductor is in accumulation. (c) After pulse is removed, remnant polarization allows inversion of the semiconductor ("on" state). (d) After depolarizing pulse, the semiconductor is depleted ("off" state).

voltage is applied to the stack such that the part of the voltage which drops across the ferroelectric is significantly greater than the coercive voltage for that layer. Figure 2.12 (b) illustrates the energy band situation for an "on" state write pulse. During the "on" state write pulse, the semiconductor is momentarily in accumulation. When the pulse is removed, and the source and gate are at the same voltage again, the voltage drop in the ferroelectric that arises due to the remnant polarization is opposed by the voltage drop across the semiconductor and insulator layers. Figure 2.12 (c) shows the case for the "on" state of the device. In this case there is sufficient band bending in the semiconductor for inversion. Setting $V = 0$ in Eq. 2.24 shows that in this case (when the source and the gate are shorted) the voltage on the ferroelectric is E_{DEPOL} (proportional to the ferroelectric polarization) reduced by some function of the relative dielectric constants of the materials in the stack.

$$V_{FE} = -\frac{E_{DEPOL}}{\frac{\epsilon_{IS}}{\epsilon_{FE} d_{IS}} + \frac{1}{d_{FE}}}. \tag{2.25}$$

It is evident from Eq. 2.25 that a higher ϵ_{IS} and a smaller d_{IS} reduces the effect of the insulating layers on the polarization of the ferroelectric and thus makes it possible in this case to invert the semiconductor channel at a lower voltage, and improve the on/off ratio of the device. Figure 2.12 (d) shows the case following an "off" state write pulse. The "off" state write pulse is close to the coercive voltage and the reduction of the polarization of the ferroelectric reduces V_{FE} such that the band bending in the semiconductor is too slight to invert the semiconductor; rather, the semiconductor surface is in depletion.

The other problem facing MFISFET devices is gate leakage. Ferroelectric polarization attracts electron injection towards the ferroelectric/insulator interface from both the gate electrode and the semiconductor channel. Electron injection and trapping in the dielectric stack causes local charge compensation in the ferroelectric, reducing the polarization. Insulating buffer layers on both sides of the ferroelectric layer can reduce this problem, but would increase the depolarization field and the

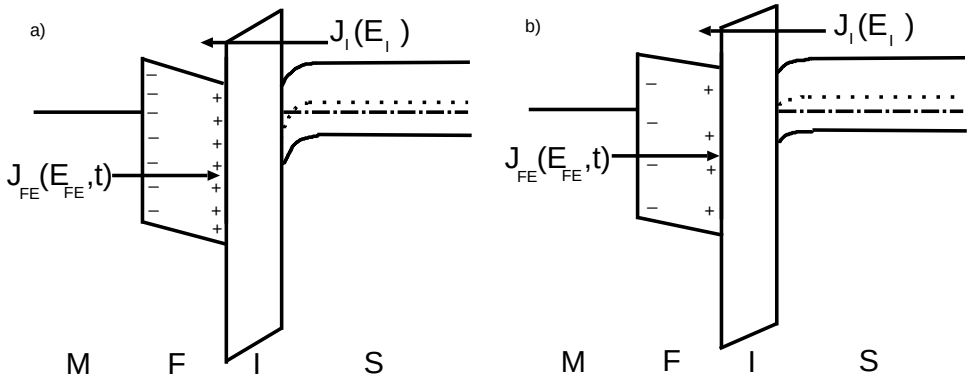

Figure 2.13: Gate leakage effects in MFIS devices. (a) Inverted semiconductor immediately after polarization, and (b) depolarization after time.

applied field necessary to polarize the device. Figure 2.13 illustrates depolarization due to gate leakage, which is time dependent. Gate leakage must be minimal for the realization of non-volatile FEFET memory. [44, 46]

One solution to both the depolarization field and leakage current is to find a high dielectric constant ferroelectric with an appropriate band alignment which can be grown as a single crystal on Si without interacting with the substrate. Since this material has not yet been found, many researchers have presented ways to reduce depolarization and gate leakage in other types of FEFETs.

To circumvent Si interface problems, other semiconductors have been proposed for use as the substrate and channel layer, to eliminate the need for a buffer layer. Epitaxial, all-perovskite devices have been fabricated. [47, 48] They have had low on-off ratios (196) and retention times of up to 8 hours.

Prins *et al.* have proposed a depletion-mode FEFET which uses an ultra thin channel layer in order to achieve complete depletion of the channel. [49] Complete depletion can be achieved when the areal charge density needed to deplete the channel is less than the remnant charge of the polarized ferroelectric. Also, band bending in the semiconductor should be minimized in order to prevent depolarization. These condi-

tions put tight restrictions on the semiconductor dopant density and the thickness of the channel layer.

For all of Prins's devices, gate leakage disturbs the device characteristics at low voltages. For channels that are very thick and have high sheet resistance, negative gate voltage drops across the semiconductor layer and not across the ferroelectric. For a thicker channel with lower sheet resistance, proper ferroelectric hysteresis is demonstrated, but the maximum on-off ratio is 7000.

2.5 Conclusions

This chapter provides an overview of ferroelectric materials and device properties. The current state of the technology for ferroelectric capacitors and ferroelectric memory devices is discussed with particular attention paid to perovskite ferroelectrics in MFIS capacitors used in FRAM and FEFETs. Fabrication and application to current silicon-based technology is briefly summarized.

3. EXPERIMENTAL TECHNIQUE

The experimental technique and procedure for fabricating and characterizing ferroelectric thin film devices is described in this chapter. First, thin film deposition and processing methods, including sputtering, chemical solution deposition, evaporation, and post-deposition annealing, are discussed. This is followed by a description of the electrical tests used to characterize ferroelectric capacitors. Dielectric, capacitance, and polarization testing equipment and theory are described.

3.1 Materials deposition

This section contains information on the methods and tools used to deposit ferroelectric thin films and conducting contacts for ferroelectric capacitors. A description of RF and ion beam sputtering is given, as well as an explanation of chemical solution deposition. This is followed by a discussion of evaporation, and an explanation of the necessity and method of post-deposition thermal processing.

3.1.1 Sputtering

Sputtering is a physical vapor deposition (PVD) technique [50, 51], which is often preferred to other PVD methods because it is possible to closely control film properties such as thickness, density, and uniformity by adjusting processing parameters including pressure, power, substrate heat and bias, and by choosing target size, stoichiometry and target- substrate distance.

Sputtering occurs when a particle is ejected from a ceramic or metallic solid target when the target is bombarded by energetic ions. The particle ejected from the target is then transported to the substrate where it condenses to form a thin film. Several methods have been developed for generating the incident ions, including ion beam and glow-discharge. For this thesis research, ferroelectric films are deposited

using an RF magnetron sputtering system, which uses a glow-discharge to generate the sputtering ions.

A glow-discharge is a self-sustaining partially ionized gas. Ar gas is commonly used as a sputter gas, and O_2 may also be used when it is desirable to incorporate oxygen into the growing film. A glow-discharge is created in the space between a positively charged anode and a negatively charged cathode. The space is filled with the sputter gas (Ar), at low pressure (<1 Torr). When a free electron enters the space, it is accelerated by the field toward the anode. Under these conditions, the mean free path of the electron is sufficiently long that it can build up enough kinetic energy to undergo an inelastic collision that excites or ionizes an Ar atom. Excited orbital electrons subsequently return to their ground state, emitting photons. This de-excitation mechanism causes the glow-discharge to glow. A collision that results in ionization creates a positively charged Ar^+ ion and another free electron.

In a self-sustaining discharge (one in which there are sufficient free electrons to maintain the discharge), electrons near the cathode are rapidly accelerated away from the cathode, and the Ar^+ ions are accelerated (more slowly) toward the cathode. When a target is placed at the cathode, the Ar^+ ions sputter the target. At any time, there are more Ar^+ ions than electrons in the space near the cathode, and this imbalance makes the glow less bright in the area near the cathode (the Crookes dark space).

AC sputtering was developed to sputter insulating materials. Insulators cannot be sputtered in DC systems because the sputtered insulating material builds up on the electrodes, making it impossible to maintain a negative bias on the cathode, and therefore impossible to sustain the glow discharge. An RF discharge is typically maintained with a 13.56 MHz AC signal.

A magnetron sputtering system incorporates a magnetic field over the cathode, which keeps electrons ejected from the target in orbits near the target surface. The field is usually generated by permanent magnets placed behind the target. A charged

particle (ion or electron) with charge q, and velocity v, in the presence of a magnetic field B, experiences a force $F = q(v \times B)$ which is normal to both the direction of travel and the magnetic field. When no other forces act on the particle, it moves in a circular path with a radius proportional to the mass of the particle. The positive Ar^+ ions have enough mass that the radius of the path is much larger than the system dimensions and they travel in straight paths across the dark space to the target.

The small mass of electrons make them strongly influenced by the magnetic field. An electron ejected from the target surface can become trapped in an orbit near the target surface, greatly increasing its path length. The increased path length of the electron makes it available for more collisions, which sustain the glow-discharge. Because electrons are thus affected by the magnetic field, the discharge in a magnetron system can be sustained at lower pressures than in other systems. The lower operating pressure of the system increases the mean free path of the particles from the target that are deposited on the substrate. This increases the deposition rate, as well as allowing the particles to reach the substrate with more kinetic energy which can improve film properties (e.g. film density).

Another sputtering system in the OSU EECS solid-state processing laboratory uses a DC discharge as an ion source. A collimated beam of ions is directed at the sputter target by an ion gun. [52]

3.1.2 Chemical solution deposition

Recently, chemical solution deposition (CSD) techniques have become popular as a means of depositing a thin film. In a typical CSD process, a solution containing the constituents of the desired film is applied to a substrate, then dried or heat-treated to drive out the solvent and obtain a solid film. Solutions are commonly, but not necessarily, organic. The most common means of applying the solution to the substrate is by spin-coating [18, 33, 53, 54], although dip-coating [34], misting, and even painting [55] have been reported.

CSD has gained favor over other means of thin film deposition because it takes only minutes to coat many substrates, film composition can be changed easily by varying the solution, and film thickness and uniformity can be controlled by using multiple coats or changing the viscosity of the solution. It is a simple matter to step up to larger substrates by using more solution.

To prepare a substrate for spin-coating, the surface must be made hydrophillic so that the liquid solution will adhere to the substrate. This is accomplished by cleaning the glass or In_2O_3:Sn, ITO,-coated slides in the Branson 5500 ultrasonic cleaner. The cleaning cycle is 30 minutes at a cleaning solution temperature of 45 °C. The solution is 5 percent Contrad70 cleaning solution in 2.5 gallons of de-ionized water.

To spin-coat a film, the solution is deposited through a filter onto the center of the substrate, which is held by vacuum to a spin chuck. The filter keeps particles (e.g. dust, precipitates) which may have gotten into the solution from getting in the film, thereby causing device failure. The spin chuck then rotates at a fast rate ($\sim$ 3000 rpm). Centrifugal force uniformly disperses the solution over the entire substrate surface. This is followed by spinning at a slower rate to begin drying the film.

The spin-dried film is tacky, and dust in the work environment or firing furnace can be incorporated into the film if care is not taken to prevent it. Cleanliness in the spin-coating work area is important for high device yield.

After spinning, films are dried further on a hot-plate or in an oven, or the solvents are fired out in a hot furnace. This can be followed by spinning on another coat, or by a final annealing process, usually at a higher temperature than the drying step, to obtain a crystalline film.

In choosing precursor materials for the solution, one must consider that they should have a high concentration of the desired element or compound, should thermally decompose without excess evaporation of the desired element or compound, and should be chemically compatible with one another. The solvents must have a

proper boiling point, and desired viscosity and surface tension. The resulting solution should have a sufficiently high concentration of the necessary components for the film. Often, an additive, such as ethylene glycol can be used to condition the solution to prevent cracking and decrease the surface texture in the finished film. [18]

The ease of mixing up a new solution compared to fabricating a new sputtering target makes CSD ideal for investigations on the effects of doping [31], or film composition. [13]

Spin-coating of photo-resist has been used for many years in integrated circuit fabrication technology, but the simplicity and cost-effectiveness of CSD makes it a popular choice for depositing many different kinds of thin films.

3.1.3 Annealing

Annealing is a necessary step in the fabrication of ferroelectric films and devices. [50] Annealing in a furnace or in a rapid thermal processing system can improve film crystallinity and stoichiometry. Ferroelectric films must be heated to assure that the film crystallizes in the appropriate phase for optimum ferroelectric (polarization) and dielectric behavior.

A box furnace uses refractory coils with an alternating current passed through them to heat the chamber in atmosphere. Ramp times in this system are limited by the ability of these coils to heat up the chamber. A box furnace is used in the research for this thesis primarily to burn the solvents out of the wet spin-coated film, and to crystallize the film.

Rapid thermal processing system (RTP) uses halogen lamps to heat a quartz processing chamber. Ramp times in the RTP are 30 seconds or less. The film temperature is monitored by thermocouple sensors. Process gases pass through the chamber during the process. An advantage of RTP is the ability to control the process environment. Samples can be annealed in pure Ar to exclude or remove oxygen from the

sample, or they can be annealed in pure O_2 in order to incorporate oxygen into the crystallizing film. After the desired ramp and soak time, the chamber is air cooled.

3.1.4 Evaporation

Thermal evaporation is a simple PVD process in which a material is heated until it melts and evaporates or sublimates. Evaporants are placed in a twisted wire "basket" or in a thin, narrow sheet of metal with a "dimple" in it to accommodate the evaporant (boat). The boat or the basket is made of a refractory metal (W, Ta, or Mo). A crucible can be placed in a basket or a ceramic-lined boat may be used when the evaporant is at risk to alloy with the metal basket or boat.

The material is heated by current passed through the basket or boat. Evaporation is usually performed at low pressures ($\leq 10^{-6}$ Torr). Under these conditions, the mean free path of the evaporant particles is longer than the distance to the substrate, so transport of the material to the substrate is line-of-sight, and film thickness and uniformity are controllable. In the work for this thesis, Au, Al, and Ni metal contacts are thermally evaporated.

Active reactive evaporation (ARE) uses a glow-discharge to disassociate gas molecules (e.g. O_2) into reactive species. ARE with an oxygen discharge can be used to oxidize metal films as they grow, and is used in this thesis research to grow In_2O_3:Sn (ITO) and SnO films from In and Sn metals.

3.2 Device characterization

In this section, methods of characterizing ferroelectric devices are discussed. Dielectric testing of PZT is described, as well as the method for extracting the Q-V hysteresis loop. All devices produced for this thesis are capacitors based on the MFM structure discussed in Chapter 2. The device structure for most of the devices is shown in Fig. 3.1 The bottom electrode is commercially available ITO-coated glass slides (1 in^2), or thermally evaporated Ni on glass. The ferroelectric film is deposited by RF

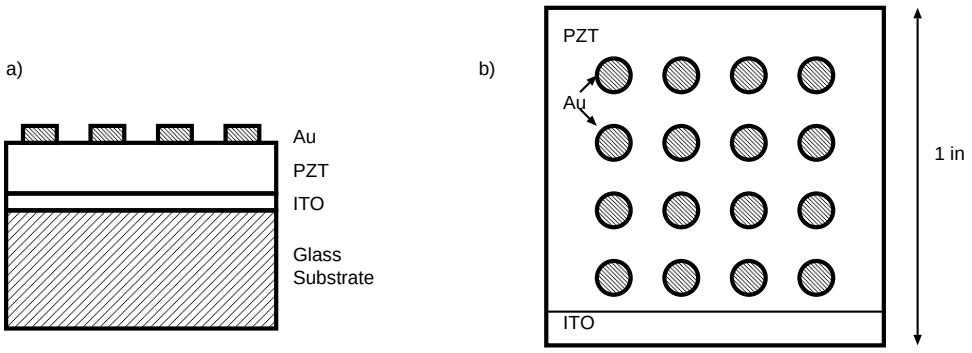

Figure 3.1: Cross-section (a) and top view (b) of ferroelectric ITO/PZT/Au capacitors.

sputtering or CSD, and annealed. Top contacts are deposited through a shadow mask by thermal evaporation or ARE, defining the capacitor area.

3.2.1 Dielectric testing

Ferroelectric materials are lossy dielectrics, which means that they have a nonzero conductivity, and that the high dielectric constant of these materials deteriorates as frequency increases. Since the ability of these materials to polarize quickly is important to their use in memory applications, it is important to have information on the frequency dependence of the dielectric behavior. Figure 3.2 shows a comparison in the frequency dependence between a lossy dielectric (PZT) and a common dielectric (SiO_2). The near lossless dielectric constant (SiO_2) has almost no imaginary part and does not vary with frequency. The magnitudes of the real and imaginary parts of the PZT dielectric constant vary with frequency.

Capacitance and conductance measurements are taken as a function of signal frequency for a small AC signal with no DC bias. From this data, and the known area A and thickness d of the film, the dielectric constant and loss tangent of the material are determined. The complex dielectric constant is described by

$$\epsilon_C = \epsilon[1 - j\frac{\sigma}{\omega\epsilon}], \tag{3.1}$$

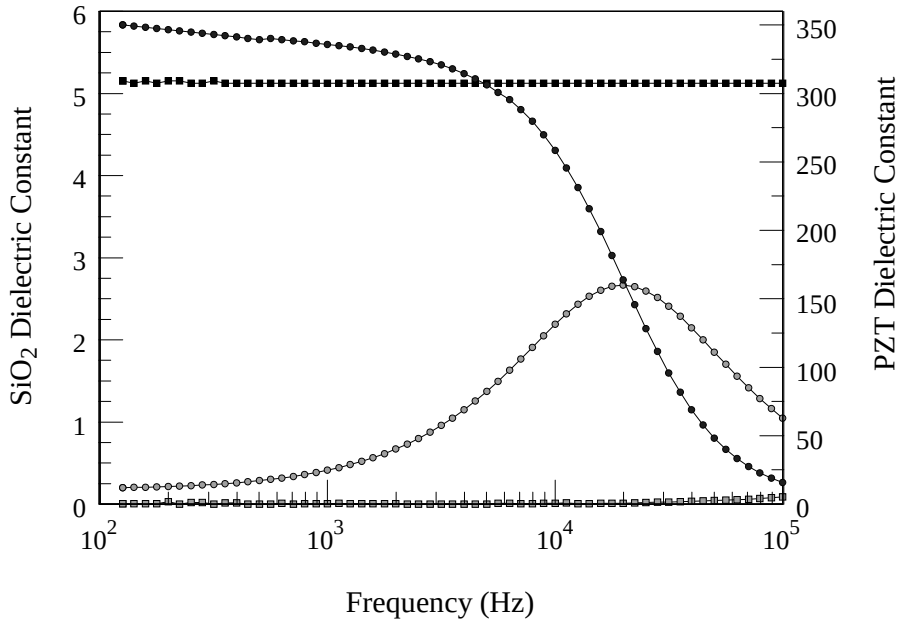

Figure 3.2: Frequency dependence of PZT (circles) and SiO_2 (squares) real (black) and imaginary (gray) parts of the dielectric constant.

Where the conductivity, σ, and the permittivity, ϵ, are both dependent on frequency. The real part of the permittivity is obtained from the capacitance by

$$C = \frac{\epsilon_0 \epsilon' A}{d}, \epsilon' = \frac{Cd}{A\epsilon_0}. \tag{3.2}$$

The conductivity is obtained from the measured conductance by

$$G = \frac{\sigma A}{d}, \sigma = \frac{Gd}{A}. \tag{3.3}$$

Then, the imaginary part of the complex dielectric constant can be obtained by using Eq. 3.3 for the conductivity in Eq. 3.1,

$$\epsilon'' = \frac{Gd}{A\omega\epsilon_0}. \tag{3.4}$$

Additionally, the loss tangent can then be calculated from the ratio of the imaginary part to the real part of the dielectric constant (ϵ''/ϵ'), or from the measured

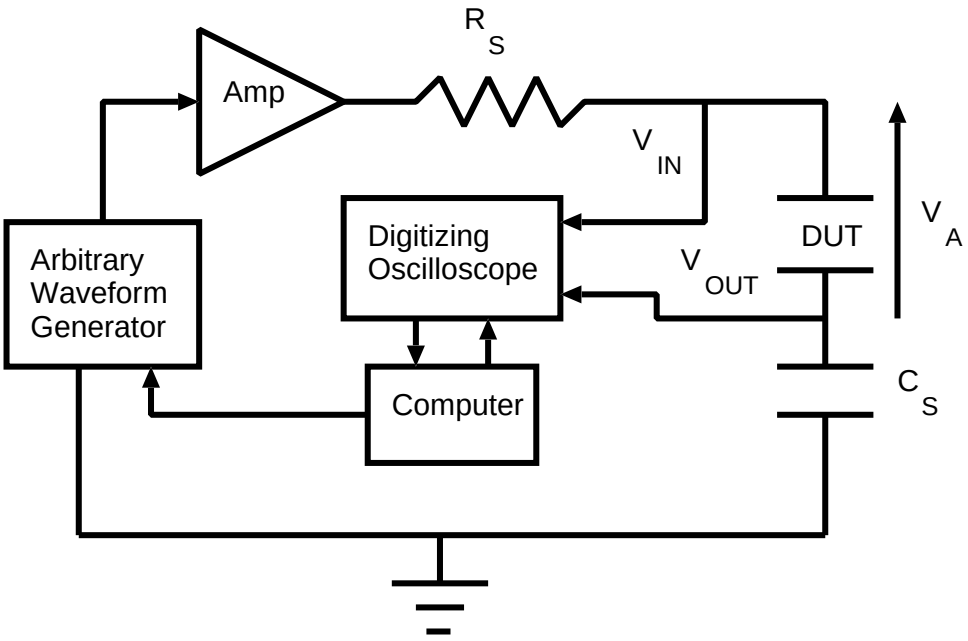

Figure 3.3: Sawyer-Tower circuit used for ferroelectric device characterization.

capacitance and conductance,

$$tan\delta = \frac{G}{C\omega}. \tag{3.5}$$

3.2.2 Polarization testing

Charge-voltage (Q-V) or polarization-electric field (P-E) measurements are obtained using a Sawyer-Tower test circuit. [7] The Sawyer-Tower circuit configuration used in the work for this thesis was originally developed for characterization of alternating-current thin-film electroluminescent devices [56] and modified to accommodate ferroelectric devices. The Sawyer-Tower test circuit is shown in Fig. 3.3

The ferroelectric device under test (DUT) is placed in series with a sense capacitor C_S and a resistor R_S (to limit current to the device). A computer-controlled waveform generator (Wavetek model 395) supplies an AC signal to an amplifier with a gain of 48, which supplies the signal to the DUT. The voltage at the input and the

output of the DUT is measured using a digital oscilloscope (Tektronix TDS 420) and is sent to the computer for analysis.

The capacitance of the sense capacitor must be significantly larger than the capacitance of the device under test to minimize its affect on the measurement. For a ferroelectric capacitor with a device area of 0.079 cm^2, a dielectric constant of 400, and a thickness of 500 nm, the capacitance is 56 nF, so that a 1 μF sense capacitor is used.

The external charge on the sense capacitor, which is the same as the external charge on the DUT, is calculated from the value of the sense capacitor and the voltage measured across the sense capacitor,

$$q = C_S V_{OUT}. \tag{3.6}$$

The voltage applied to the DUT is the difference between the voltage measured at the input and the output of the DUT,

$$V_A = V_{IN} - V_{OUT}. \tag{3.7}$$

The polarization (or charge per unit area) is calculated by dividing the total charge by the area of the device. The electric field is calculated by dividing the applied voltage by the thickness of the device. A typical P-E hysteresis loop is shown in Fig. 2.3.

3.3 Conclusions

This chapter contains a description of the experimental procedure and characterization technique used for the investigation of ferroelectric capacitors. First, an overview of materials deposition processes including sputtering, CSD, evaporation, and annealing is given. This is followed by a description of the device structure and methods of device characterization. Dielectric, capacitance, and polarization testing procedures are described with particular attention paid to the frequency dependence of the dielectric constant of lossy dielectrics.

4. FERROELECTRIC CAPACITORS

Since the ultimate goal of this project is to fabricate transparent ferroelectric capacitors, the first step in this process is the fabrication and characterization of non-transparent ferroelectric capacitors. This is accomplished by depositing the ferroelectric layer either by sputtering or by chemical solution deposition (CSD) specifically, by spin-coating. The first capacitors discussed in this chapter are ones for which the ferroelectric layer is deposited by RF sputtering. This is followed by a section on capacitors for which the ferroelectric layer is spin-coated. Next, a novel ferroelectric device is discussed which has a NiO layer next to the spin-coated ferroelectric layer. This is followed by a discussion of preliminary results for transparent ferroelectric devices, including devices with transparent contacts, and devices which include an insulating buffer layer. The final section of this chapter contains conclusions regarding transparent and non-transparent ferroelectric capacitor development.

4.1 Ferroelectric capacitors by RF sputtering

This section contains a description of the fabrication of ferroelectric devices for which the ferroelectric layer is deposited by RF sputtering. Process parameters for ferroelectric thin film deposition are explained first, followed by discussions of the dielectric and polarization versus electric field (P-E) data.

4.1.1 Capacitor fabrication

Ferroelectric PZT MFM capacitors are fabricated by depositing PZT by RF sputtering onto commercial ITO-coated substrates. After deposition, PZT films are annealed and metal top contacts are evaporated through a shadow mask which defines the device area.

The ITO-coated substrates are cleaned in a Branson 5500 ultrasonic cleaner in a solution of 5 percent Contrad70 detergent in de-ionized (DI) water. The ultrasonic

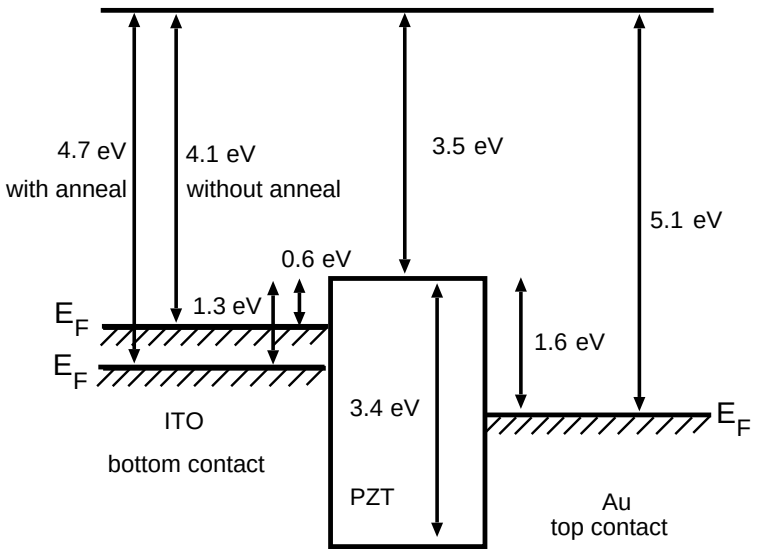

Figure 4.1: The barrier to electron injection from ITO can be improved by annealing.

cycle is 30 minutes long and the solution is heated to 45°C before the cycle begins. The cleaned substrates are rinsed with DI water and annealed in an RTP system at 300°C in oxygen. This post-cleaning anneal serves two purposes. First, it removes the water which is absorbed in the substrate from the cleaning solution and the DI rinse, and second, it fills some of the oxygen vacancies in the ITO, making it slightly less conductive, but also slightly increasing the work function of the ITO layer. As illustrated in Fig. 4.1, increasing the work function of this layer increases the barrier to electron injection into the PZT, and may help reduce leakage current due to Schottky emission of electrons.

The PZT layer is deposited by RF sputtering a 2 in. diameter target of $Pb(Zr_{0.52},Ti_{0.48})O_3$, purchased from Alfa Aesar. The target is sputtered at 70 watts to achieve a desirable deposition rate. The substrates are heated to 150°C before deposition. This substrate temperature is sufficient to reduce thermal stress on the film which may cause cracking. Using higher substrate temperature reduces the de-

position rate. The target-to-substrate distance is about 2 in. Increasing this distance decreases the deposition rate.

The chamber pressure is kept at 10 mTorr during film deposition. Films deposited at this pressure have significantly higher dielectric constants than films deposited at higher pressures. This is most likely due to improved film density at lower pressures rather than an improvement of crystallinity, since films are not crystallized in the perovskite form until they are annealed after deposition. The constituents of the target sputter at different rates at different pressures. At 10 mTorr, Pb seems to sputter much slower than the other target constituents. If the target is sputtered for a long time at this pressure, films become Pb-deficient and conductive. Consistently good film quality can be achieved by pre-sputtering the target at 30 mTorr for an hour prior to a device film deposition. The ambient gas flow rate in the chamber is 40 sccm Ar and 10 sccm O_2. This allows sufficient oxygen to be incorporated into the film.

Substrates are moved very slowly (0.045 in./minute) past the target during deposition. Substrates pass the target twice, once going in each direction. This improves film uniformity. When three substrates are placed on the substrate holder, the deposition takes four hours. The thicknesses of the resulting films are measured using and AlphaStep 500 profilometer. Most of the sputtered films for this work are $\sim$500 nm thick.

As-sputtered films are amber in color, indicating that a PbO phase remains. [57] Films are annealed at 650°C by RTP in O_2 to form the perovskite phase. After anneal, the films are transparent with a slight yellow tint, and appear cloudy due to surface texture.

Metallic top electrodes are evaporated onto the PZT layer by thermal evaporation through a shadow mask. The electrodes are circles, each with an area of 0.079 cm^2. These define the device area. Au or Ni metal electrodes are thermally

evaporated in a Veeco evaporation system, and Al metal electrodes are evaporated in a Polaron thermal evaporation system.

Au and Ni have high work functions, i.e. 5.1 eV and 5.2 eV, respectively, so that the barrier to electron injection is high and the devices can be polarized with a high electric field before electrons are injected and current flows freely through the device (device breakdown). Al has a work function of 4.3 eV which means that the barrier to electron injection is not very high, only ∼0.8 eV. Remarkably, devices with Al top electrodes can also be polarized with a high field before they break down. This is mostly likely due to the fact that Al oxidizes easily. A thin layer of aluminum oxide forms at the PZT/Al interface, which reduces leakage current and does not appreciably affect the dielectric and P-E properties of the device.

4.1.2 Dielectric properties

The most important figure of merit for these devices is the dielectric constant at a frequency of 1 kHz. This is the same signal frequency used for the P-E measurement, which is discussed in the following section. Figure 4.2 is a plot of the real and imaginary parts of the dielectric constant as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF sputtering. The dielectric constant at 1 kHz for this device is 353.

The dielectric data are derived from capacitance and conductance measurements. Figure 4.3 is a plot of the capacitance as a function of frequency for this device. The real part of the dielectric constant, ϵ', is directly proportional to the capacitance, $\epsilon' = Cd/A\epsilon_0$. Note in Fig. 4.2 that the real part of the dielectric constant diminishes significantly above 10^4 Hz. This is because the capacitance decreases at this same frequency.

The conductance as a function of frequency is plotted in Fig. 4.4. The imaginary part of the dielectric constant, ϵ'', is directly proportional to conductance and inversely proportional to the frequency, $\epsilon'' = Gd/A\epsilon_0\omega$. The conductance of this de-

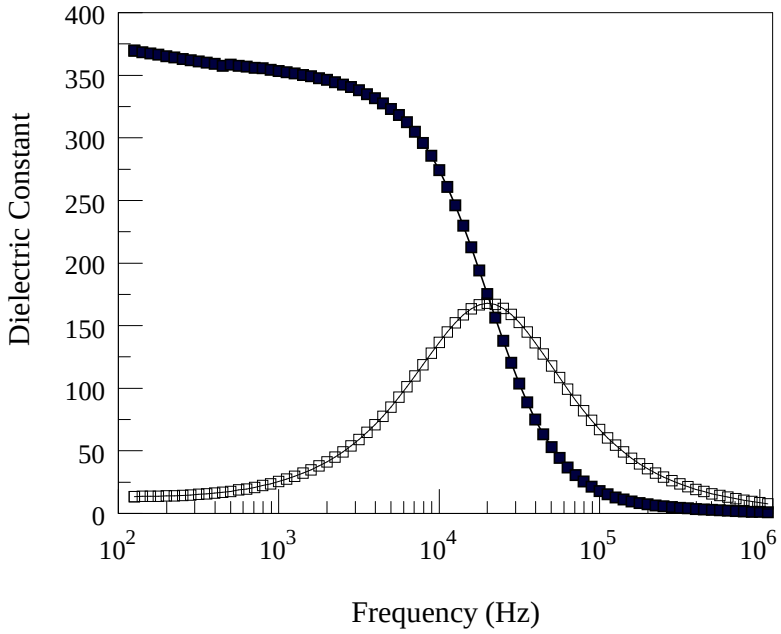

Figure 4.2: Real (filled) and imaginary (open) parts of the dielectric constant as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering.

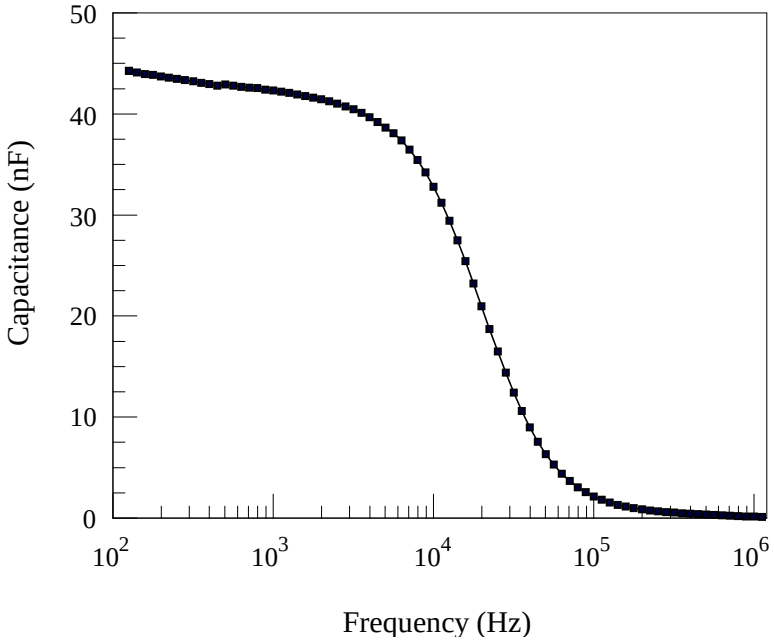

Figure 4.3: Capacitance as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering.

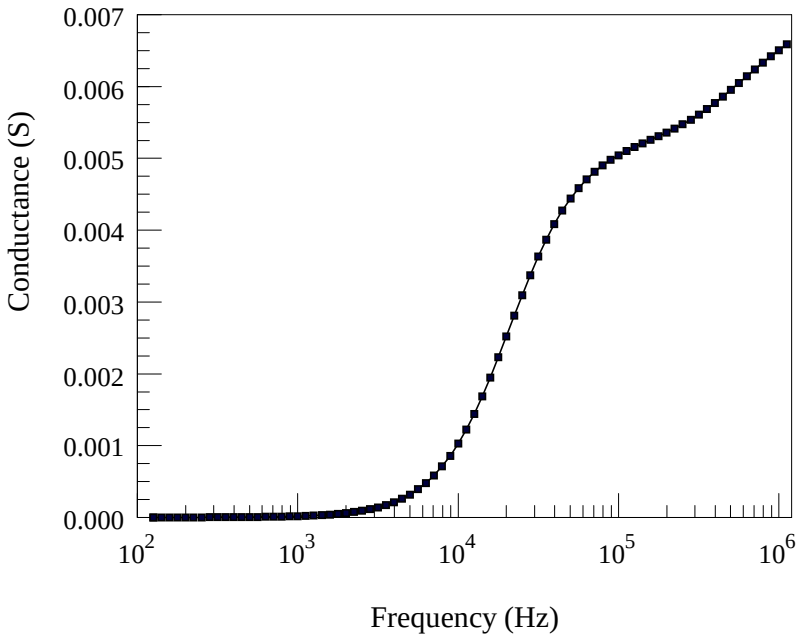

Figure 4.4: Conductance as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering.

vice at 1 kHz is 19.2 μS, indicating that some current flows through this device, even though only a small AC bias is applied.

The loss tangent of a capacitor is the ratio of the imaginary to the real part of the dielectric constant, ϵ''/ϵ', which is plotted in Fig. 4.5. At low frequencies, the real part of the dielectric constant is much larger than the imaginary part of the dielectric constant, so the loss tangent is small at low frequencies. At 10^4 Hz, the imaginary part of the dielectric constant becomes significant compared to the real part, so the loss tangent increases at this point. At high frequencies, both parts of the dielectric constant are small, so the ratio of the imaginary to the real part of the dielectric constant (loss tangent) stays high.

The highest yield obtained for PZT capacitors deposited by RF sputtering is 10 out of 16 working devices, with some substrates exhibiting no working devices.

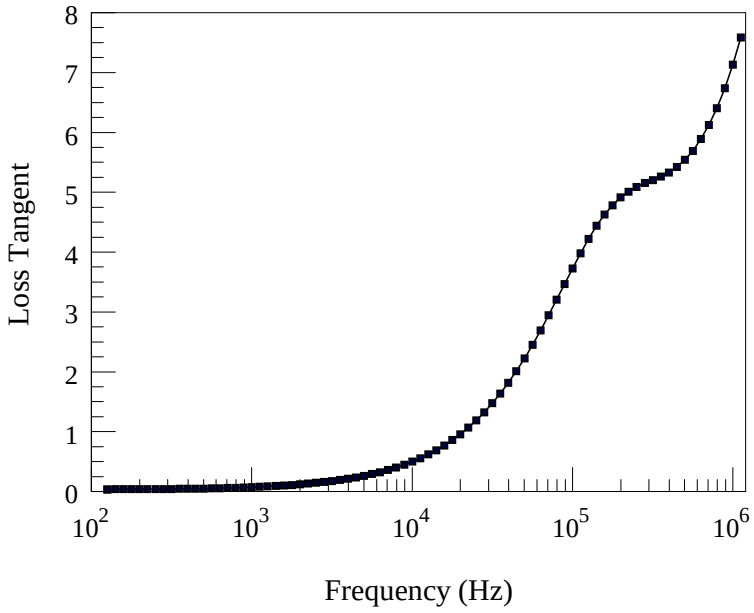

Figure 4.5: Loss tangent as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering.

Yield is improved by taking care that the target is pre-sputtered at 30 mTorr prior to sputtering a device film.

4.1.3 Polarization properties

The dielectric properties of PZT capacitors discussed in this thesis are measured with no applied DC bias, and meaningful dielectric data can be obtained as long as the electrode is sufficiently conductive and the PZT is sufficiently insulating. Polarization properties of ferroelectric capacitors are assessed using P-E analysis. P-E data are taken at a constant measurement frequency of 1 kHz different applied field strengths. Some ferroelectric capacitors exhibit too much leakage current even at low applied field strength for their polarization properties to be measured. Thus, dielectric data can often be obtained even for devices for which no P-E data can be obtained.

A P-E plot for an ideal ferroelectric capacitor is shown in Fig. 4.6. The parts

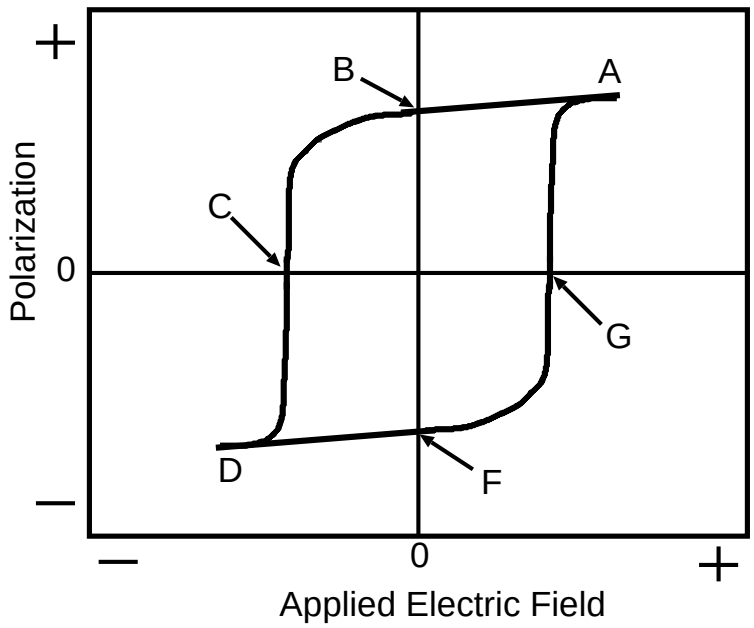

Figure 4.6: P-E plot for an ideal ferroelectric capacitor.

of the plot labelled A and D represent the spontaneous polarization of the device in the + and - maximum field directions, respectively. B and F indicate remnant polarization, and C and G indicate the negative and positive coercive fields.

When a device is spontaneously polarized in the + field direction (A), a positive voltage is applied to the top electrode. For an ITO/PZT/Au capacitor, this is the Au electrode. Figure 4.7 shows an energy band diagram for a capacitor thus biased. In this situation, the ferroelectric switching charge, Q_{FS}, and the ordinary dielectric polarization charge, Q_{DP}, are arranged in a manner to oppose the applied voltage, which is established by the charge due to the applied voltage, Q_{AP}. The charge due to the applied field is due to free charges at both of the metal/ferroelectric interfaces. The application of a positive polarizing voltage results in an applied field, which induces ferroelectric switching.

When the applied voltage is removed, which is indicated by the line from A to B in Fig. 4.6, there is no applied voltage induced charge. Q_{DP} becomes negligible, but

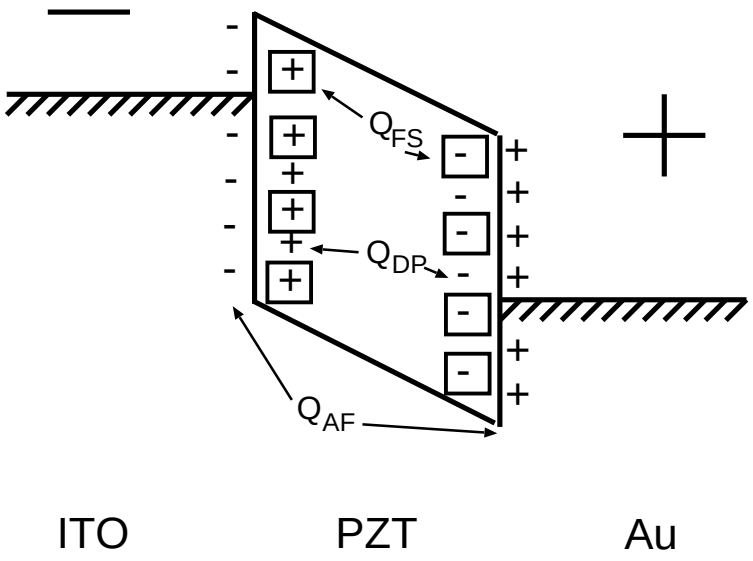

Figure 4.7: ITO/PZT/Au capacitor which is spontaneously polarized by a positive voltage applied to the Au electrode. Charge due to applied field, Q_{AF}, charge due to ordinary dielectric polarization, Q_{DP}, and charge due to ferroelectric switching, Q_{FS}, are indicated.

Q_{FS} is persistent, so that the free charge on the plates remains. Since this charge is not due to an applied voltage, it is termed "remnant" charge, Q_R, and is associated with the large remnant polarization of the ferroelectric material when the applied voltage is removed. This situation is illustrated in Fig. 4.8.

Point C in Fig. 4.6 corresponds to the negative coercive field of the ideal device. The coercive field is defined as the point at which half of the ferroelectric switching charge has changed direction.[1] Figure 4.9 shows an energy band diagram for this situation. If the curve at C is nearly vertical, then the coercive field is well defined, meaning that most of the ferroelectric switching occurs at a single value of the applied field.

Point D in Fig. 4.6 is similar to point A, except that the polarizing field is in the opposite direction, i.e. the Au contact is negatively biased. Point F is similar to B, and G is similar to C, except that the polarizing field is in the opposite direction.

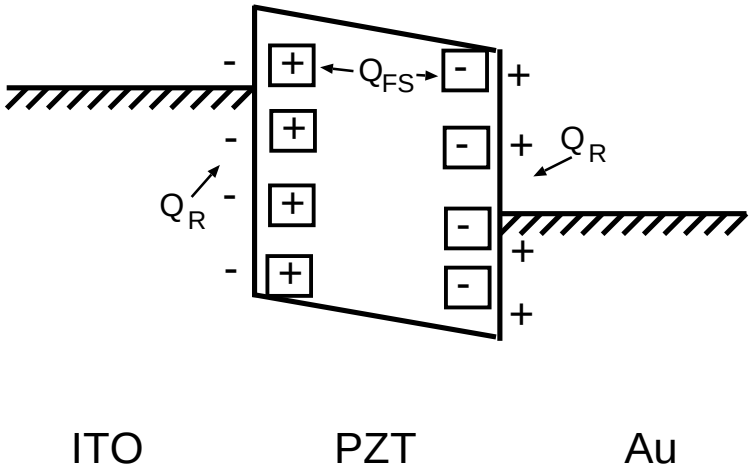

Figure 4.8: ITO/PZT/Au capacitor showing a remnant polarization after the application and removal of a polarizing voltage pulse. Charge due to ferroelectric switching, Q_{FS}, and induced remnant charge on the electrodes, Q_R, are indicated.

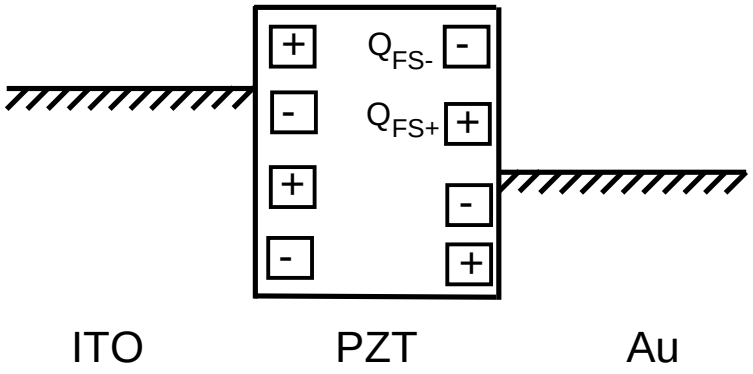

Figure 4.9: ITO/PZT/Au capacitor at its coercive field value. Half of ferroelectric switching charge, Q_{FS}, is in + direction, and half is in - direction.

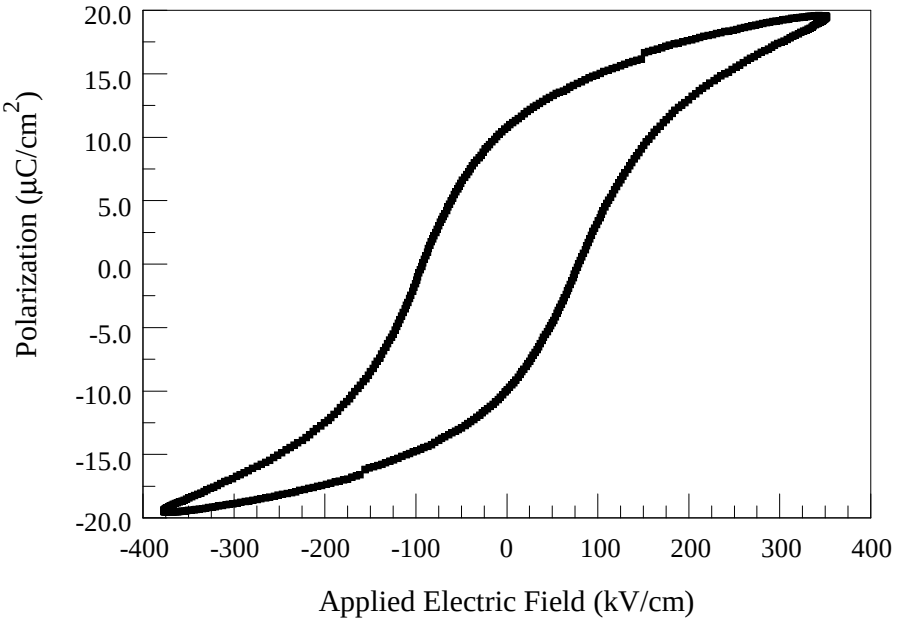

Figure 4.10: Polarization versus applied electric field for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering.

An important attribute of the ideal P-E curve is that the slopes of lines AB and CD should be as close to zero as possible, indicating that all of the ferroelectric charge is switched and that ferroelectric switching is dominant. The slopes of the curve near C and G should be close to infinity, to insure that ferroelectric switching is abrupt. A high slope of line AB or CD implies that a significant amount of the polarization at point A is due to charge which is not Q_{FS} or Q_{DP}, and may be due to charge injection and trapping in the ferroelectric layer. A decrease from ideality of the slope near G and C might again be due to charge injection and trapping, or may indicate non-crystallinity of the ferroelectric film. Variations in film crystallinity throughout the film may cause variations in the amount of voltage required to polarize the ferroelectric switching charge.

The P-E data for the same device whose dielectric data are discussed in the previous section is given in Fig. 4.10. This device shows favorable, symmetric

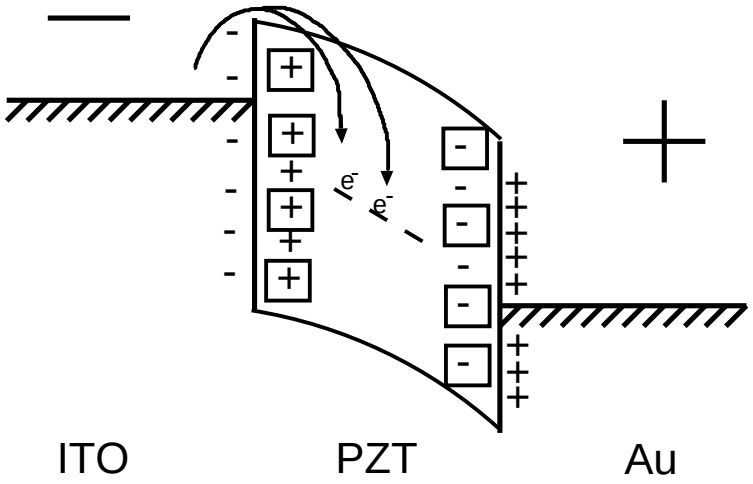

Figure 4.11: Electron injection into the PZT and subsequent electron trapping. Note that such electron trapping results in a nonuniform electric field across the PZT layer.

properties in that the coercive fields have similar magnitudes in the + and - field directions, 80 kV/cm and 100 kV/cm, respectively. The remnant polarization and spontaneous polarization values are similar in both field directions, $P_R = +11$ and -10.8 μC/cm^2, and $P = +20$ and -20 μC/cm^2. The remnant polarization for this device is only 55 percent of the spontaneous polarization. This results in a hysteresis loop that is not square; the slopes of the lines which correspond to AB and DF on Fig. 4.6 are quite high, and the slopes near the coercive field values, C and G, are low (not infinite) indicating the existence of charge in the film which is not due to ferroelectric switching, and has greater magnitude than ordinary dielectric polarization alone. This additional charge is probably due to injection and trapping of charge in PZT layer.

Figure 4.11 illustrates one possible mechanism for charge trapping in the PZT layer. Traps in the PZT are filled at various field strengths, as electrons are able to surmount the injection barrier via Schottky emission from the ITO electrode. Electron injection and trapping is more likely to occur when a positive field is applied to the Au side of the capacitor, since the barrier for electron injection from ITO is much lower

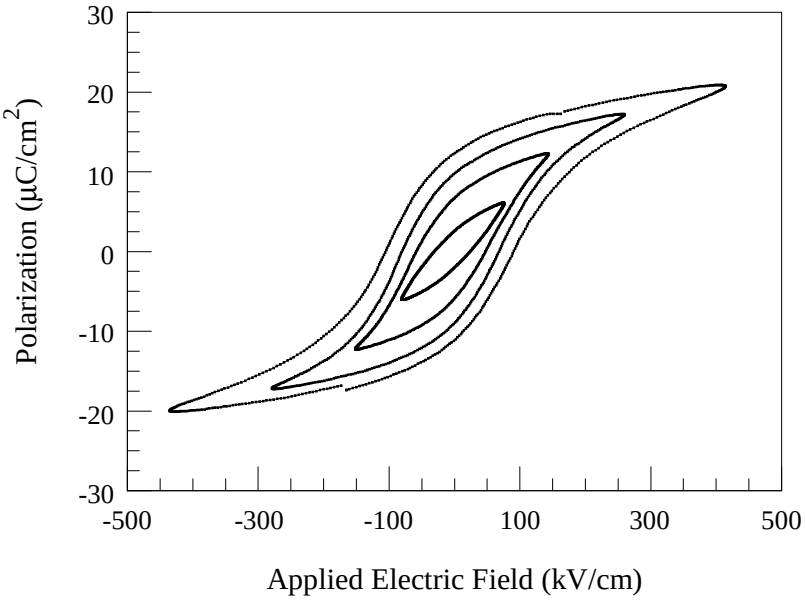

Figure 4.12: Polarization versus applied electric field for an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF magnetron sputtering, at varying maximum electric field strength.

than from Au. When electron injection and trapping occurs, not all of the polarization charge monitored in a P-E measurement actually arises from ferroelectric switching. Electron trapping results in a nonuniform electric field across the PZT layer. When the applied field polarity is reversed, electron emission from traps can occur; higher fields lead to higher electron emission rates. Device breakdown can occur when the extent of electron trapping becomes too great.

Figure 4.12 illustrates how P-E curves evolve as the applied field strength increases. At applied fields below the coercive field, the device does not exhibit ferroelectric hysteresis. The smallest curve in Fig. 4.12 shows what one would expect to see for a linear, lossy capacitor. [1] For this curve hysteresis is attributed to the lossy nature of the device, rather than to ferroelectric switching, since the curve shows little evidence of ferroelectric switching, i.e., the coercive field regions

indicated as C and G in Fig. 4.6. As the field increases, the P-E curve begins to form a square hysteresis loop, indicating ferroelectric switching; eventually the polarization begins to approach saturation. Near device breakdown, i.e., the outside loop, a significant amount of charge moves within the ferroelectric layer, most likely due to electron injection from the ITO electrode. As this injected electron charge moves within the PZT layer due the field, which is applied as a sine wave, it causes the voltage measured at the sense capacitor of the Sawyer-Tower circuit to shift during the measurement, which appears as a break in the P-E plot. The output voltage is measured in two sections. First, the positive half of the sense capacitor output voltage is captured at some instant, while the applied voltage continues to change. After the positive waveform is captured, the negative half of the sense capacitor output voltage is captured. Since the positive and negative portions of the output voltage waveform are not captured in direct succession, any change in the DC output voltage, due to charge rearrangement in the PZT film between measurements, appears as a DC shift in the P-E loop, giving rise to a distinct break in the P-E curve. Thus, the presence of such a break in the P-E curve is experimental evidence of the onset of breakdown. This is a useful diagnostic attribute of a P-E curve.

Table 4.1 summarizes the polarization properties for the ITO/PZT/Au capacitor which is discussed in this section, for which the PZT layer was deposited by RF sputtering. The similarities in the + and - polarization properties are evident in the table, underscoring the symmetrical nature of this ferroelectric capacitor. Also note that the coercive voltages for this device are near 5 V, a reasonable value for use in current semiconductor applications.

4.1.4 Conclusions

The fabrication and properties of an ITO/PZT/Au capacitor for which the PZT layer is deposited by RF sputtering are discussed in this section. Such ferroelectric MFM capacitors exhibit high dielectric constant and good symmetrical polarization

Table 4.1: Polarization properties for an ITO/PZT/Au ferroelectric capacitor.

Sample	0505031
Back contact	ITO
PZT thickness	580 nm
Top contact	Au
ϵ	353
tan δ	0.072
$+V_C(V)$	5.0
$-V_C(V)$	5.7
$+P$ (μC/cm^2)	20
$-P$ (μC/cm^2)	20
$+P_R$ (μC/cm^2)	11
$-P_R$ (μC/cm^2)	10.8

properties, indicating that RF sputtering is a viable means of depositing PZT. However, composition and uniformity of these films are difficult to control, and device film depositions are time consuming, requiring several hours.

4.2 Ferroelectric capacitors by chemical solution deposition

This section contains a discussion of the fabrication and characterization of ferroelectric MFM capacitors for which the ferroelectric layer is deposited by CSD, specifically, by spin-coating. The development of the spin solution is discussed first, followed by capacitor fabrication including the spin-coating process. Then, dielectric properties of some spin-coated films are explained and P-E plots are interpreted. Finally, conclusions regarding ferroelectric capacitors for which the PZT layer is deposited by spin coating are discussed.

Table 4.2: Composition of the PZT spin solution.

Material Name	**Amount in Solution**
lead acetate	6 g
titanium isopropoxide	1.15 mL
zirconium n-propoxide (in propanol)	3.8 mL
acetic acid	3 mL
propanol	6 mL
ethylene glycol	0.3 mL

4.2.1 Solution development

The PZT precursor solution developed for this work is based on the solution developed by Yi *et al.* [18] The solution contains lead acetate (trihydrate), Zr n-propoxide (70 weight percent in propanol), Ti isopropoxide, and ethylene glycol purchased from Alfa Aesar, and propanol and acetic acid purchased from OSU Chemstores. The composition of the PZT spin solution is indicated in Table 4.2.1.

Lead acetate is measured out using a precision scale and then dissolved in acetic acid by heating and stirring on a Thermolyne hot plate with a magnetic stirrer. This solution is allowed to mix for at least thirty minutes at 80°C. Next, zirconium n-propoxide is added and mixed at 60°C for one hour. Then titanium isopropoxide is added and mixed at 60°C for one hour. It is important to mix the zirconium n-propoxide first and to allow it to mix well before adding the titanium isopropoxide in order to prevent the titanium isopropoxide from reacting with the acetic acid and forming precipitates. [18] Once the Zr and Ti are in the solution, 6 mL of propanol is added to dilute the solution, and 0.3 mL of ethylene glycol is added to condition the solution and prevent cracking when the film is fired. The complete solution is mixed at 60°C for at least an hour.

4.2.2 Capacitor fabrication

Substrate preparation is of integral importance in a CSD process. Since the solution is spun-on, the surface of the substrate must be hydrophillic to allow the solution to adhere to the substrate. The substrates used to fabricate the spin-coated capacitors are the same ITO-coated Corning 1737 glass slides which are used as back contacts for the RF-sputtered capacitors. These substrates are cleaned and dried in the same manner as the ones which are used to fabricate RF sputtered devices. It is the ultrasonic cleaning cycle which makes the surface of the ITO hydrophillic.

A small amount of solution is filtered and applied to the clean, dry substrate surface, and then spun at 3000 rpm for 60 seconds to form a smooth film. The sample then spins at 500 rpm for 60 seconds to begin drying the film. The resulting tacky film is then placed in a 500°C furnace to fire out the solvents and begin crystallizing the film. After being removed (cool) from the furnace, either another coat is applied and fired using the same procedure, or the film is annealed (by RTP) at 650°C in oxygen. The thickness of the final film is measured using a profilometer.

The 60 second spin and dry times are established from an experiment which determines spin parameters that avoid film cracking when the film is deposited on glass. Films with 60 second spin and dry times are found to be least likely to crack, owing to the fact that they are thinner than films that are not spun and dried as long. Shorter spin and dry times may make a film which is less dry when it is put into the firing furnace, and some of the spin-induced surface texture may level out. Using thinner (more dilute) spin solutions also reduces spin-induced surface texture.

Films for this thesis consist of one, two, or three coats with a final thickness between 400 and 700 nm. Within experimental error it cannot be determined from the data in this thesis whether two or more coats improves film quality. It is true that in applying multiple coats, the opportunity for the inclusion of particles in the film increases, and data for this thesis indicates that yield diminishes when more than two coats are applied.

If the film is removed from the firing furnace before it cools, the rapid cooling of the film causes it to crack. Using very thin layers may reduce the stress on the film, but then many layers have to be deposited to make a film of desired thickness.

Metal top contacts which define the MFM device area are applied to the films by evaporation in the same manner to which they are applied to the RF-sputtered films. Ni, Au, and Al are thermally evaporated. Transparent conductive oxide films have been applied as top contacts to CSD-derived films. The results of these processes are discussed further in Section 4.4 of this thesis.

4.2.3 Dielectric properties

Figures 4.13 and 4.14 show plots of dielectric constant versus film thickness for films deposited by RF sputtering, by 1-coat spin-coating, and by 2-coat spin coating. The data in Fig. 4.13 are for capacitors with ITO bottom contacts and Au top contacts. In Fig. 4.14 data is shown for MFM capacitors with ITO bottom contacts and Au, Ni, ITO, or Al top contacts.

Two trends are evident from these figures. First, the dielectric constant of the films increases with film thickness. Second, the spin-coated films tend to have higher dielectric constant than the RF sputtered films even when the thicknesses are comparable. This may be due to the fact that the Zr/Ti ratio for the two processes is different, or may be an indication that better crystallinity is achieved with the spin-coating process.

Figures 4.13 and 4.14 indicate that there is a tendency for the 2-coat spin-coated films to have higher dielectric constants than the 1-coat films. This is largely due to the 2-coat films being thicker. Thicker films can only be achieved with multiple coats, if cracking is to be avoided.

The spin-coated film which had the highest dielectric constant with acceptable conductance is a 730 nm thick 2-coat film. The dielectric constant is 695 and the conductance is 54 μS. Figure 4.15 is the dielectric constant plot for this device.

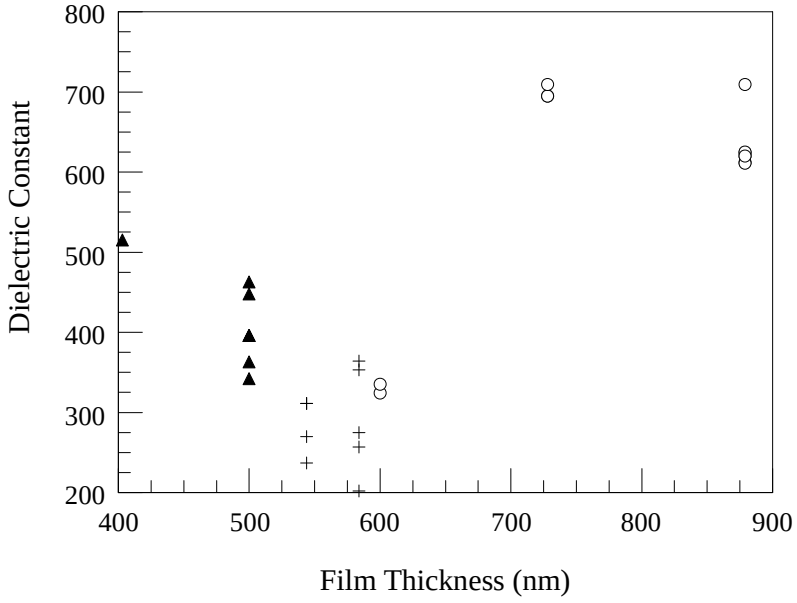

Figure 4.13: Dielectric constant versus thickness for RF sputtered (crosses), 1-coat spin-coated (triangles), and 2-coat spin-coated (circles) PZT films with Au top contacts.

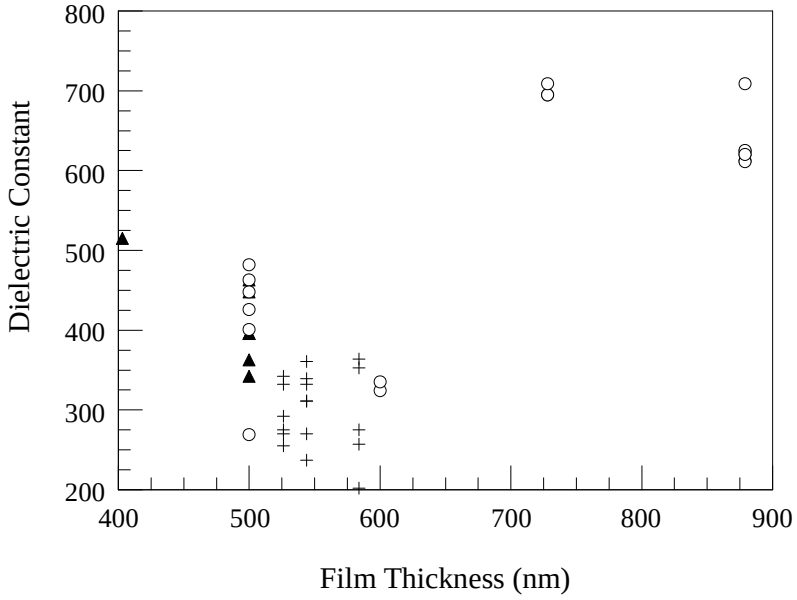

Figure 4.14: Dielectric constant versus thickness for RF sputtered (crosses), 1-coat spin-coated (triangles), and 2-coat spin-coated (circles) PZT films with various types of top contact.

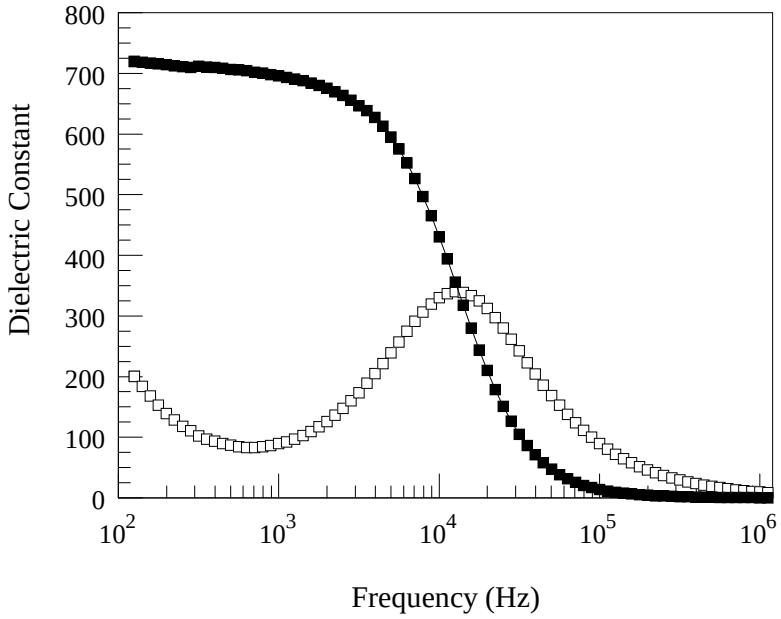

Figure 4.15: Real (filled) and imaginary (open) parts of the dielectric constant as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by spin-coating. The PZT thickness is 730 nm.

The high dielectric constant is due to the thickness of the film. It is a common trait of ferroelectrics that the dielectric constant is thickness-dependent. The higher conductance of this device at 1 kHz with respect to the RF sputtered device discussed in Sect. 4.1 is evident by comparing ϵ'' at 1 kHz in Fig. 4.15 to ϵ'' at 1 kHz in Fig. 4.2, since G is directly proportional to ϵ'', $G = \epsilon'' A\epsilon_0\omega/d$.

The real part of the dielectric constant, and also the capacitance, starts to diminish at a lower frequency in this device than in the device for which the PZT is sputtered. This may be an indication of the crystallinity of the film, or may be due to the increased thickness of the film. The processing parameters, including firing and annealing time and temperature, are optimized for a film which is 500 nm thick (two 250 nm thick coats). These parameters may be insufficient to fully crystallize a

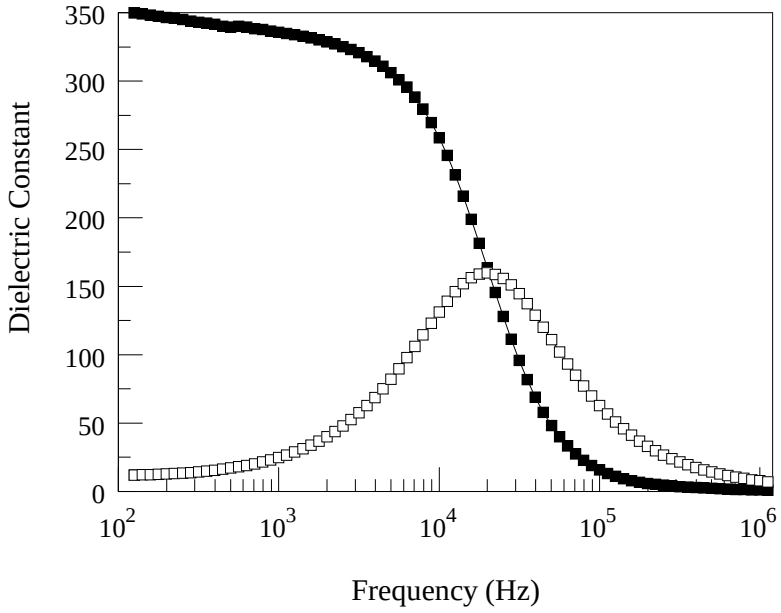

Figure 4.16: Real (filled) and imaginary (open) parts of the dielectric constant as a function of frequency for an ITO/PZT/Au capacitor for which the PZT layer is deposited by spin-coating. The PZT thickness is 600 nm.

730 nm thick film, with each coat more than 350 nm thick, or the firing cycle may not fully remove all of the solvent, leaving defects in the film.

For more direct comparison to the MFM capacitor examined in Sect. 4.1, consider the dielectric constant plot shown in Fig. 4.16. This figure is remarkably similar to Fig. 4.2. The two devices have similar dielectric constants, 353 for the RF sputtered capacitor, and 335 for the spin-coated capacitor, and similar conductance, 19.2 μC for the RF sputtered capacitor, and 18.2 μC for the spin-coated capacitor. The differences in these devices are more evident in the polarization properties, which are examined in the next section.

4.2.4 Polarization properties

The P-E plot for the 730 nm thick PZT film discussed in the previous section is shown in Fig. 4.17. This curve has a more square shape than the P-E curve in Fig.

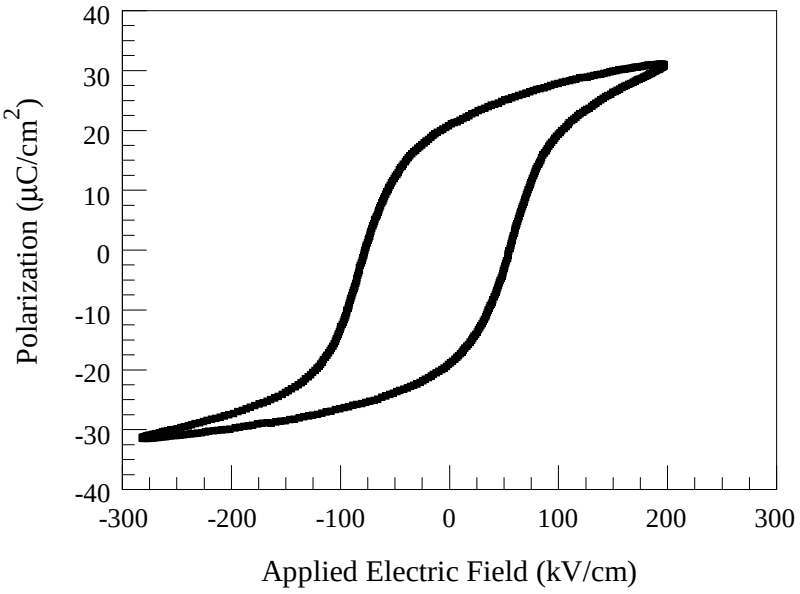

Figure 4.17: Polarization versus applied electric field for a spin-coated PZT capacitor. The PZT thickness is 730 nm.

4.10, for the RF sputtered film. The spontaneous and remnant polarization values are higher for this 730 nm thick device, as one would expect for a device with a higher dielectric constant; more charge can be stored in the same area. This thicker film has more ferroelectric dipoles than the 580 nm thick sputtered film, so the ferroelectric switching charge is larger fraction of the total charge, and therefore is not as obscured by the non-switching charge as in the thinner film. Thus, the curve has a more square (ferroelectric switching) appearance.

Non-switching charge due to ordinary dielectric polarization and charge trapping are evident in this curve, in the same way as in Fig. 4.10. The slopes of the curve between the spontaneous and remnant polarization values, corresponding to AB and DF in Fig. 4.6, are high, and the coercive fields are not well defined. Charge injection from the ITO side, when the Au is positively biased, is more evident in Fig. 4.17 than in Fig. 4.10, which may indicate that more charge is injected

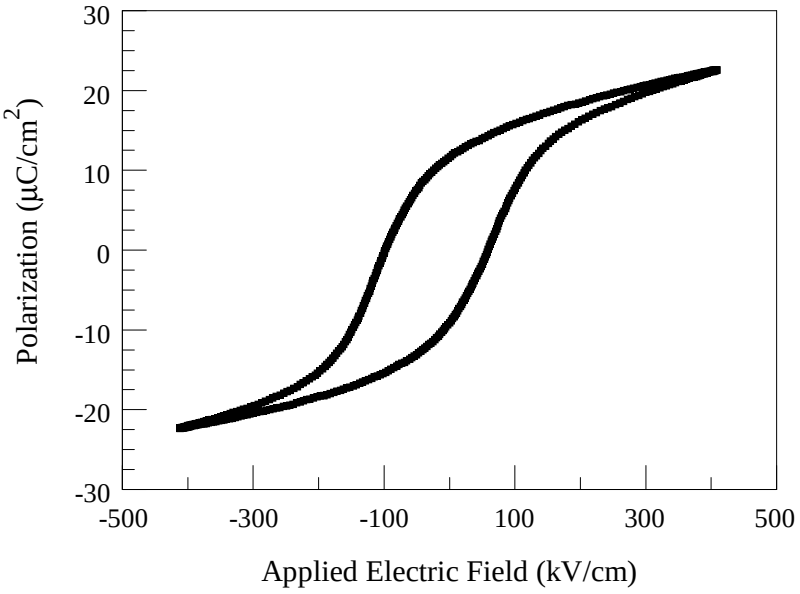

Figure 4.18: Polarization versus applied electric field for a spin-coated PZT capacitor. The PZT thickness is 600 nm.

into the thicker film. The thicker film is more conductive, which may indicate that there are more defects in the film due to non-crystallinity. These defect sites can act as electron traps. Thus, injection and trapping of electrons from the ITO electrode greater in this film than in the RF sputtered film. It may also be that there are more electron traps in this film simply because it is thicker.

Figure 4.18 shows the P-E curve for the 600 nm thick spin-coated device discussed in Sect. 4.2.3. In this case the asymmetry due to electron injection and trapping from the back electrode is less evident, which again indicates that there is more trapping in the thicker film due to increased electron trapping in that film.

It is worth noting that the ITO contacts for spin-coated devices are subjected to four thermal processes. Two thermal processes take place in O_2 ambient (pre-deposition and final anneal in RTP), and two take place in an air ambient (firing each coat). This thermal processing makes the ITO contact for spin-coated films less

Table 4.3: Polarization properties for ITO/PZT/Au capacitors.

Sample	0723032	0702033	0505031
Back contact	ITO	ITO	ITO
PZT thickness	730 nm	600 nm	580 nm
PZT deposition	spin-coated	spin-coated	RF sputtered
Top contact	Au	Au	Au
ϵ	695	335	353
tan δ	0.128	0.061	0.072
$+V_C$ (V)	4.0	3.4	5.0
$-V_C$ (V)	5.0	5.9	5.7
$+P$ (μC/cm^2)	30	22	20
$-P$ (μC/cm^2)	30	22	20
$+P_R$ (μC/cm^2)	22	11.7	11
$-P_R$ (μC/cm^2)	20	8.8	10.8

conductive than the ITO contact for RF sputtered films, which are only subjected to the pre-deposition and final annealing processes in the RTP. For this reason, more of the applied voltage drops across the ITO used as a contact to spin-coated PZT than RF sputtered PZT, and more voltage must be applied to fully polarize capacitors with spin-coated PZT layers.

The polarization properties for the three MFM capacitors discussed in this chapter are summarized in Table 4.3.

4.2.5 Conclusions

ITO/PZT/Au capacitors for which the PZT layer is deposited by spin-coating are demonstrated in this section. The capacitors exhibit high dielectric constant, higher for thicker films. The composition of these films is easy to control by altering

the relative quantities of precursors in the spin solution. Device film deposition takes only a few minutes, but firing times are a few hours.

4.3 Nickel and nickel oxide capacitor

This section contains dielectric and polarization data for a novel ferroelectric capacitor structure which has an additional dielectric layer of NiO caused by the unintentional oxidation of the back Ni electrode. Device fabrication is discussed first, followed by explanations of the dielectric and polarization properties of the device.

4.3.1 Capacitor fabrication

The back contact of this device is evaporated Ni, which is often used as a top contact in this thesis research because it has a high work function (5.2 eV [35]) and low cost (compared to Au). When Ni is used as the back contact for spin-coated capacitors, the exposure to the spin solution as well as the firing and annealing processes causes the Ni back contact to oxidize, and a nickel oxide layer to grow between the Ni contact and the PZT film. The PZT layer in this device is a two-coat spin-coated film from a solution which results in a 500 nm thick PZT film. The original intent of fabricating a device with a Ni back electrode was to verify whether failure of a capacitor with a top ITO electrode was due solely to the properties of the ITO which is deposited as the top electrode, or if it was due to both electrodes being ITO. All Ni/NiO/PZT/ITO capacitors failed; current flow through the devices at low applied field made P-E properties impossible to measure. Thus, evaporated Al is used as a top contact to verify that the Ni/NiO/PZT/ITO devices failed because of the top ITO, and not because of the PZT layer. As discussed in Sect. 4.1, Al forms a very thin oxide layer at the PZT/Al interface which reduces leakage current and has no discernable effect on the dielectric and polarization properties of the device.

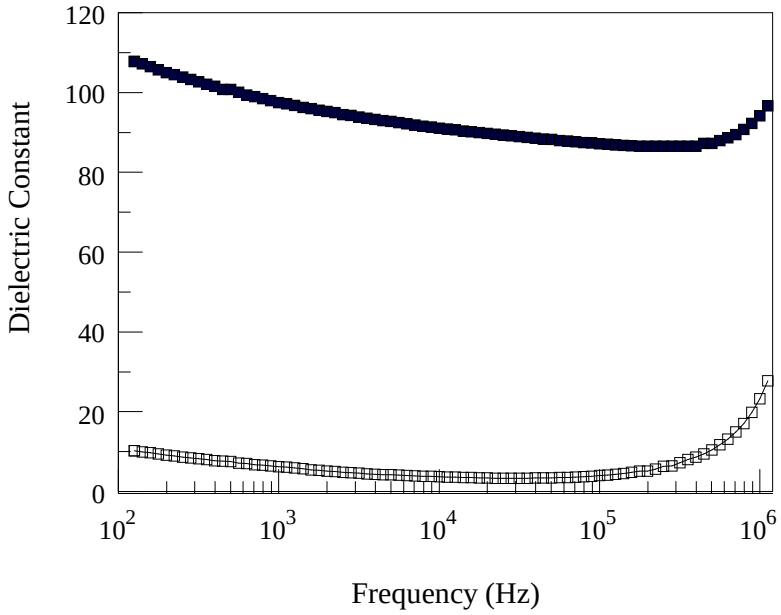

Figure 4.19: Real (filled) and imaginary (open) parts of the dielectric constant as a function of frequency for a spin-coated PZT capacitor with a NiO layer.

4.3.2 Dielectric properties

Figure 4.19 shows the dielectric behavior for the Ni/NiO/PZT/Al capacitor. The real and imaginary parts of the dielectric constant follow the same trend, and remain relatively constant as a function of frequency, much like the dielectric data for SiO_2, which is discussed in Sect. 3.2. Since the dielectric data are not frequency-dependent, this has the appearance of a near-lossless dielectric. The real part of the dielectric constant at 1 kHz is 97.5, nearly 10 times the dielectric constant of NiO alone, which is 12. [58] 97.5 is slightly less than a third of the dielectric constant of similar PZT films on ITO. Thus, ϵ' for this ferroelectric capacitor appears to arise from a series combination of the PZT and NiO dielectrics. Assuming this to be the case, an approximate value for the thickness of the NiO layer can be calculated from

the formula for capacitors in series,

$$\frac{1}{C_{EFF}} = \frac{1}{C_{NiO}} + \frac{1}{C_{PZT}}. \tag{4.1}$$

$C = \epsilon/d$ can be substituted in to Eq. 4.1, since all areas are equal,

$$\frac{d_{EFF}}{\epsilon_{EFF}} = \frac{d_{NiO}}{\epsilon_{NiO}} + \frac{d_{PZT}}{\epsilon_{PZT}}. \tag{4.2}$$

Substituting $d_{PZT} + d_{NiO}$ for the effective thickness and solving for d_{NiO},

$$d_{NiO} = \frac{d_{PZT}}{1 - \frac{\epsilon_{EFF}}{\epsilon_{NiO}}}(\frac{\epsilon_{EFF}}{\epsilon_{PZT}} - 1). \tag{4.3}$$

The effective dielectric constant is 97.5, d_{PZT} and ϵ_{PZT} are assumed from the thickness and dielectric constants of other films made from the same solution. ϵ_{NiO} is assumed to be 12, from reference [58]. In this case, the NiO layer is approximately 48 nm thick. This value for the thickness of the NiO layer seems high. Other reasons for the decrease in dielectric constant compared to PZT on ITO have to be considered. It is possible that PZT does not easily form in the perovskite phase on Ni, or NiO, and the non-crystallinity of the PZT layer may reduce the dielectric constant. Also, it is likely that the NiO and PZT layers are not completely separate, and some mixing has occurred during the thermal processing.

4.3.3 Polarization properties

The P-E curve for the Ni/NiO/PZT/Al capacitor is shown in Fig. 4.20. The P-E loop is relatively square, with remnant polarization 71 and 69 percent of the spontaneous polarization. In this device, when the top contact, Al, is positively biased, as it is in the upper right part of the P-E plot, a large barrier to hole injection from the Al side exists, and a large barrier to electron injection from the Ni side exists. This case is depicted in Fig. 4.21 (b). Polarization of the PZT layer is induced by the applied field and no charge is due to charge injection. This is why the slope of the curve which corresponds to AB in Fig. 4.6 is small.

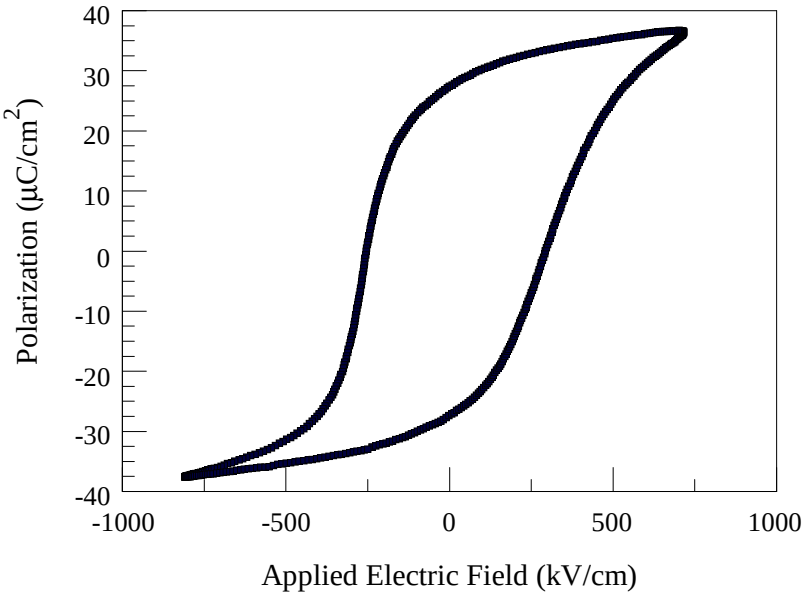

Figure 4.20: Polarization versus applied electric field for a Ni/NiO/PZT/Al capacitor.

The case when the Al side is negatively biased is depicted in Fig. 4.21 (c). In this case, which corresponds to the lower left part of Fig. 4.20, holes are easily injected into the NiO from the Ni electrode and electrons are easily injected into the PZT from the Al electrode, and the effect of the polarization due to the applied field is enhanced.

The polarization values are higher in this device than in the ITO/PZT/Au devices, because this capacitor is less conductive. The conductance of this device at 1 kHz is only 5.5 μS, so very little of the polarization due to the applied field is compensated by current flow through the device.

4.3.4 Conclusions

This section contains a demonstration of a novel ferroelectric Ni/NiO/PZT/Al capacitor for which the PZT layer is deposited by spin-coating and a NiO layer is unintentionally formed due to thermal processing of the PZT layer. The unique

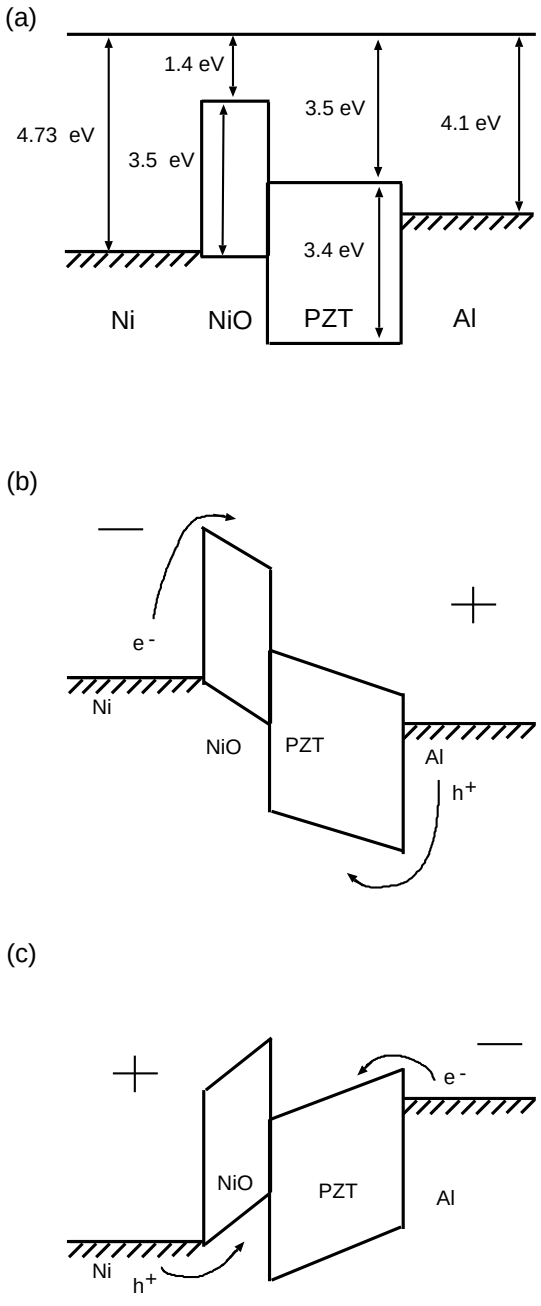

Figure 4.21: Energy band diagrams for and Ni/NiO/PZT/Al capacitor.

Table 4.4: Polarization properties for a Ni/NiO/PZT/Al capacitor.

Sample	NiPZTAl
Back contact	Ni/NiO
PZT thickness	500 nm
Top contact	Al
ϵ	97.5
tan δ	0.064
$+E_C$	16 V
$-E_C$	14 V
$+P$	38 μC/cm^2
$-P$	39 μC/cm^2
$+P_R$	27 μC/cm^2
$-P_R$	27 μC/cm^2

dielectric and polarization properties of this device are discussed. While this device is not applicable to the goals of this project, interpreting the data derived from this device provides a better understanding of the effects of charge injection and trapping in ferroelectric capacitors.

4.4 Transparent ferroelectric capacitors

Since the ultimate goal of the project initiated with this thesis research is to fabricate Pb-free, fully transparent ferroelectric capacitors for FRAM and FEFET memories, this section contains some preliminary transparent PZT capacitor results. First, properties of ITO/PZT/Au capacitors, for which the PZT layer is deposited under the same processing parameters, are discussed for comparison purposes. Next,

ITO and In_2O_3/Ga_2O_3 (IGO) are discussed as transparent top contacts to PZT. Finally, CaF_2 and HfO_2 insulating buffer layers are discussed.

4.4.1 Film fabrication

The PZT films deposited for use in the transparent ferroelectric capacitors discussed in this section are 2-coat spin-coated PZT films. The back contact is ITO, cleaned and dried in the same manner as is described in Sect. 4.1. The films are about 500 nm thick and have an expected dielectric constant near 300 at 1 kHz.

4.4.2 ITO top contacts

Many researchers have successfully deposited PZT films onto transparent ITO, as discussed in this thesis. [59, 60] Ferroelectric PZT films form in the perovskite phase on ITO after a high temperature anneal ($> 600°C$). Since an ITO-coated substrate works well as a bottom electrode, ITO is considered to be an appropriate choice for a top electrode. At OSU, ITO can be deposited by ion-beam sputtering, RF sputtering, or activated reactive evaporation (ARE).

Depositing ITO by ion-beam sputtering causes ion-induced damage to the PZT layer which must be annealed out. Annealing PZT in a reducing atmosphere, even at temperatures as low as 200°C, destroys the ferroelectric properties of the film. [61] Annealing ion-beam deposited ITO in oxygen ruins the conductive properties of the film, so it is impossible to remove ion-induced damage by annealing without ruining the PZT or the ITO film.

RF sputtering ITO also causes ion-induced damage to the PZT. RF sputtered ITO can be annealed in oxygen up to 300°C, without appreciably reducing the conductivity, but ITO/PZT/ITO capacitors with RF sputtered ITO top contacts still fail. Either a 300°C anneal is insufficient to remove the damage, or there is a problem with the quality of the ITO. It is possible that the ITO is not sufficiently dense. That the ITO deposited at OSU is less dense than commercial ITO is evidenced by the

fact that ITO deposited at OSU has a much faster wet chemical etch rate than the commercial ITO.

ITO deposited in the ARE is simply not conductive enough to be an electrode. In and Sn metals are evaporated in an activated oxygen ambient to produce an oxide film. ITO with 10 percent Sn is created by layering depositions of In and Sn. The layered film is then furnace annealed in air at 200°C for an hour to mix the layers. The thermal processing and the oxidation of Sn during deposition cause resulting films to have low conductivity.

4.4.3 IGO top contacts

Indium-gallium oxide (IGO) is deposited in the ARE by simultaneous evaporation of In and Ga sources. First, the Ga source is heated until it begins to evaporate. Once a constant rate of 0.2 Å/s is obtained, a thin (2 nm) Ga_2O_3 layer is deposited to keep the In_2O_3 out of direct contact with the PZT. As discussed in Ch. 2 of this thesis, In_2O_3 has a low work function compared to PZT, and the low barrier to electron injection may cause current leakage. Then, the In source is heated until the total rate is 1 Å/s. A 20:80 ratio of Ga_2O_3 to In_2O_3 is reported to have a work function close to 5 eV. [62] The concentration is difficult to know in the ARE, since one source is much closer to the substrates than the other.

The same processing parameters are used in the processing of every film in the ARE for this thesis research. The plasma which activates the oxygen is operated at 150 watts. The chamber pressure is maintained at 0.3 mTorr by controlling the oxygen gas flow with a leak valve. Deposition rates are kept below 1 Å/s to allow the evaporant to oxidize. Although the process parameters are kept constant, slight variations in parameters can cause vast differences in film properties, making results difficult to reproduce.

Capacitors with IGO top contacts exhibit P-E curves which indicate that the ARE-depsited IGO does not have a 5 eV work function, possibly because it is not

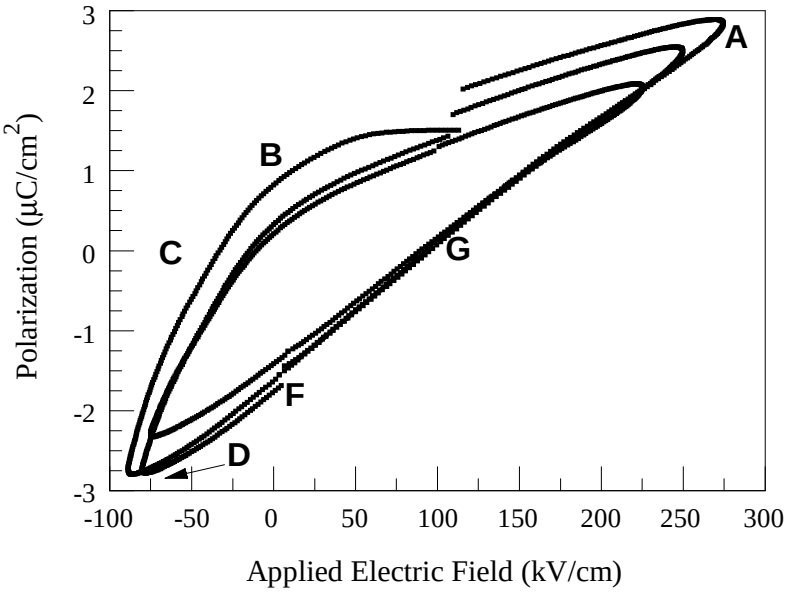

Figure 4.22: Polarization versus applied electric field for an ITO/PZT/ITO ferroelectric capacitor. The PZT layer is deposited by spin-coating.

thermally processed and deposition parameters such as evaporation rate are difficult to control in the ARE. The P-E curve is plotted in Fig. 4.22. The letters on this plot correspond to the letters on Fig. 4.6. This curve breaks down before the ferroelectric can fully polarize. The noticeable breaking points in this curve indicate that this capacitor breaks down due to charge injection. Since this occurs at a much lower applied field than similar ITO/PZT/Au capacitors, it appears that charge is injected from the IGO electrode.

The curves in Fig. 4.22 do not exhibit ferroelectric behavior. The bend in the P-E curve near point B is more likely due to diode-like charge injection from the IGO electrode, rather than to ferroelectric polarization. Figure 4.23 depicts an energy band diagram for this device, assuming that the IGO has a much lower work function than the anticipated 5 eV. Since the portion of the curve from D to A exhibits a straight-line trend, as expected for a simple capacitor, no ferroelectric

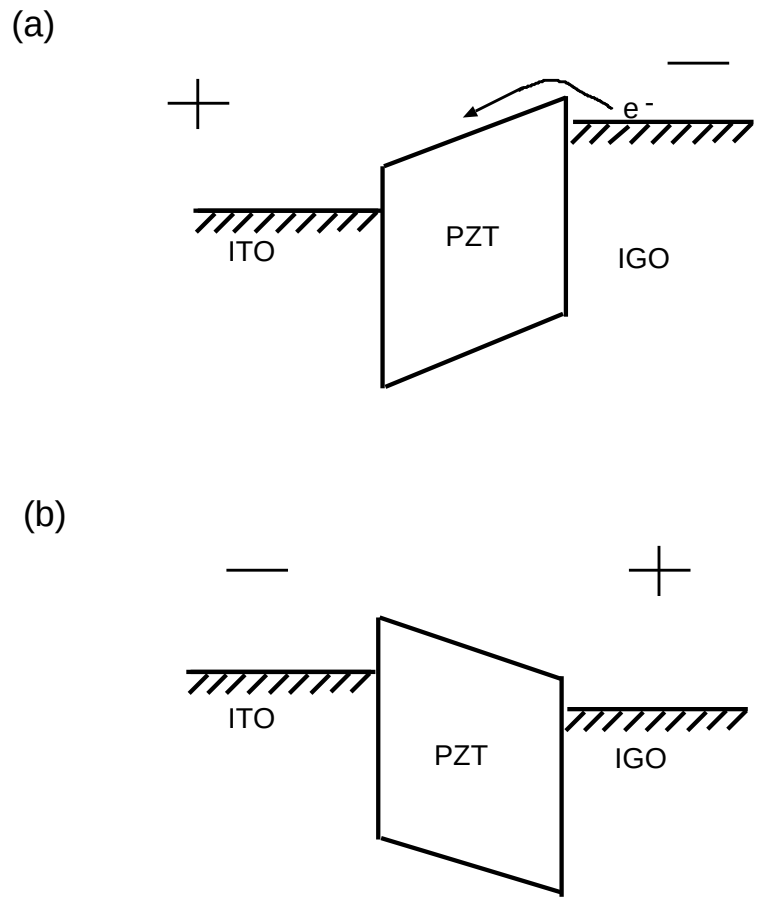

Figure 4.23: Energy band diagram for and ITO/PZT/IGO capacitor. (a) When IGO is negatively biased, electron are injection occurs from the IGO electrode into the PZT and the the device acts as a forward biased diode. (b) The magnitude of the positive bias on the IGO electrode is insufficient to result in electron injection from the ITO electrode

switching occurs in this direction. The offset of Fig. 4.22 is also indicative of diode-like behavior of this device when the IGO is negatively biased. The amplifier used in the Sawyer-Tower circuit is not designed to have a resistive load. When a resistive load is applied to the amplifier, the amplification of the input signal is reduced, and less voltage is applied to the device. Since the applied field is reduced in only the negative direction, this suggests an asymmetrical load on the amplifier. Since current flows through the ITO/PZT/IGO capacitor when a negative field is applied, the amplifier is applying a lower field in the negative direction.

4.4.4 CaF_2 insulating buffer layer

Adding a thin layer of CaF_2 before applying a MFM capacitor top contact provides promising results. After the PZT film undergoes its final anneal, a 10 nm thick CaF_2 is deposited on the PZT by thermal evaporation. CaF_2 is evaporated at a low rate to preserve the insulating nature of the film. After the CaF_2 film is deposited, ITO top contacts are deposited by RF sputtering, creating a transparent ITO/PZT/CaF_2/ITO capacitor. The RF sputtered ITO deposited by this process can be annealed at 300°C in oxygen while maintaining sufficient conductivity for use as a top electrode. This allows some of the sputter-induced damage to be annealed out while the PZT is not exposed to a reducing atmosphere.

The ITO/PZT/CaF_2/ITO capacitor exhibits hysteresis in its P-E plot, as shown in Fig. 4.24. The reference points from Fig. 4.6 are imposed on the P-E plot. The width of the P-E plot, i.e., the horizontal distance from point C to point G is due to both charge injection and the presence of the insulating layer. Some of the applied field drops on the CaF_2 layer, so a larger total field must be applied to fully polarize the PZT layer.

The effects of charge injection and ordinary dielectric charge of the CaF_2 and PZT layers are apparent in the slopes of lines AB and DF. The applied field is

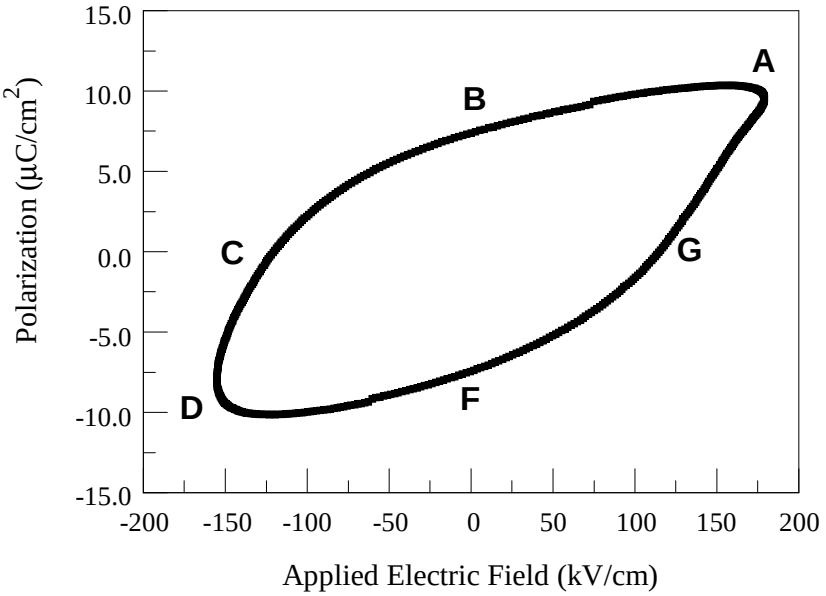

Figure 4.24: Polarization versus applied electric field for a spin-coated PZT MFIM capacitor with a 10 nm CaF_2 layer, and ITO top and bottom contacts.

not great enough to fully polarize the ferroelectric switching charges, so ferroelectric switching charges represents a small fraction of the total charge.

Breakdown in this device appears to be due to charge injection from the CaF_2/ITO electrode. The curve in Fig. 4.24 is the last curve which can be measured before the device breaks down. The breaks in the curve near B and F indicate that breakdown is due to charge injection. The applied field is smaller than would cause breakdown due to charge injection from the back ITO electrode, so breakdown appears to be due to charge injection from the CaF_2/ITO electrode. Charge injection on this side may be due to sputter damage in the CaF_2 from the top ITO electrode deposition, which may not have annealed out completely. It may also be that the CaF_2 layer is too thin to be an effective buffer layer.

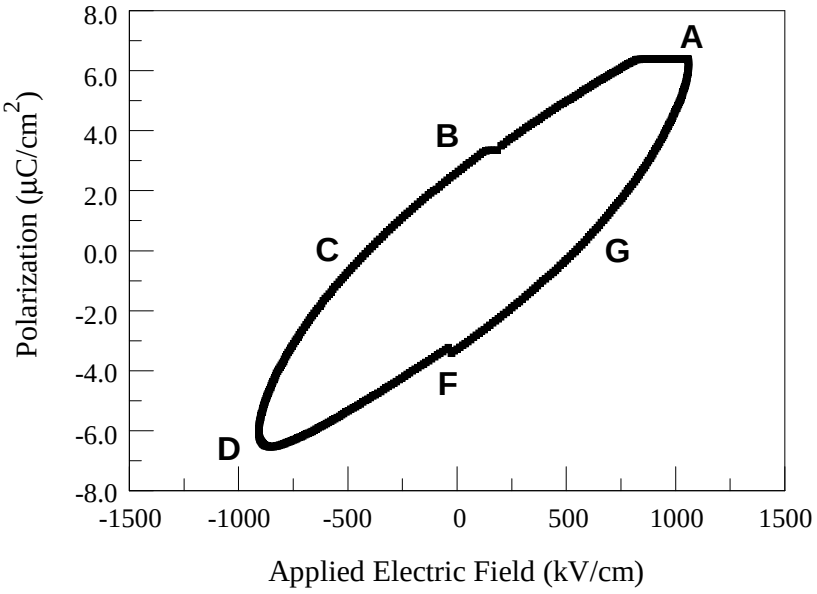

Figure 4.25: Polarization versus applied electric field for a spin-coated PZT MFIM capacitor with a 170 nm HfO_2 layer, an Al top contact and an ITO bottom contact.

4.4.5 HfO_2 insulating buffer layer

HfO_2 is another possible material for use as an insulating buffer layer for obtaining a transparent top contact to PZT. HfO_2 can be processed in the OSU EECS solid-state processing laboratory by RF sputtering. It has a high dielectric constant relative to SiO_2 ($\sim$20).

The capacitor discussed in this section consists of a 400 nm PZT film which is spin-coated onto ITO. 170 nm of HfO_2 is deposited onto the PZT by RF sputtering. Finally, Al top contacts are deposited by thermal evaporation.

The ITO/PZT/HfO_2/Al capacitor begins to exhibit hysteresis just before it breaks down. The P-E plot for this device is Fig. 4.25. The slopes of lines AB and DF are quite steep in this plot for several reasons. This is a very high applied field, and much of the voltage is dropped across the HfO_2 layer. Not enough voltage is applied to the PZT layer to fully polarize the ferroelectric switching charge, so the

ferroelectric switching charge represents a small fraction of the total charge. The ordinary dielectric charge of both the HfO_2 and PZT layers, and the injected charge, dominate the ferroelectric switching charge.

Breakdown of this device is due to charge injection, although it is not clear which side of the device is more likely to inject. That the breakdown is due to charge injection is apparent in the P-E plot where it breaks near points B and F. Injection from the HfO_2/ITO side would most likely be caused by sputter damage to the PZT layer during the HfO_2 deposition. Breakdown due to electron injection from the ITO side would be due to the high applied field, and the low barrier to electron injection at the ITO/PZT interface. HfO_2 has an electron affinity of 2.5 eV, so the barrier to electron injection into the HfO_2 from the Al electrode is 1.8 eV, according to ideal theory. [10]

4.5 Conclusions

This chapter contains data obtained from fabricating and characterizing ferroelectric PZT capacitors. First, ITO/PZT/Au capacitors for which the PZT layer is deposited by RF sputtering or by spin coating are discussed and compared. The ease and cost-effectiveness of spin-coating make it a better method for pursuing ferroelectric capacitor fabrication. Understanding the P-E and dielectric information of these MFM capacitors makes it easier to understand more complicated device structures, such as the MFIM Ni/NiO/PZT/Al capacitor, and capacitors with transparent electrodes and insulating buffer layers.

A transparent top contact must be sufficiently conductive so that very little voltage drops across it. It must have a high work function so that the barrier to electron injection is high and so that devices do not break down at fields below the coercive field, and therefore exhibit no ferroelectric hysteresis. Transparent top contacts must not require thermal processing in a reducing atmosphere to be conductive,

as such processing ruins the properties of the ferroelectric film. Deposition of transparent top contacts must not induce damage in the PZT layer due to energetic ions.

Transparent insulating buffer layers must provide a good barrier to electron injection. They must have a high dielectric constant to minimize their effect on the total voltage required to polarize the device. They must have good breakdown properties, since much of the applied voltage drops in the buffer layer. If an insulating buffer layer is present on only one side of the ferroelectric layer, asymmetric P-E curves are observed.

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

This chapter summarizes the accomplishments demonstrated in this thesis and provides recommendations for future work on ferroelectric materials and devices.

5.1 Conclusions

The ultimate, long-term goal of the project initiated in this thesis is the realization of transparent ferroelectric devices. Ideally, this would be accomplished by the fabrication of lead-free, fully transparent ferroelectric capacitors integrated with transparent thin-film transistors, or, alternatively, the fabrication of lead-free, fully transparent FEFETs. The major accomplishments of this thesis involve initial steps toward achieving this goal.

- A literature review of the fundamentals of ferroelectric devices is undertaken, as elucidated in Ch. 2 of this thesis.
- PZT is identified as an appropriate material for initiating a study of ferroelectric materials. Even though PZT is not fully transparent, it is chosen as a starting material because of its excellent ferroelectric properties, i.e., its high dielectric constant and remnant polarization. Also, much can be learned from the abundance of literature on PZT.
- Deposition methods for PZT are identified and implemented. Although both RF sputtering and spin-coating deposition are investigated, spin-coating appears to be a better method for future development of transparent ferroelectrics at OSU.
- Ferroelectric characterization techniques are identified and employed. Dielectric characterization, involving measurement of the real and imaginary parts of the dielectric constant as a function of frequency, and polarization - electric field (P-E) assessment are the two primary characterization techniques used.

The realization of a P-E measurement system involved modification of an existing computer program and a Sawyer-Tower circuit which was formerly used for alternating-current thin film electroluminescent (ACTFEL) device characterization.

- The major accomplishment of this thesis is the demonstration of capacitors which exhibit ferroelectric properties. The dielectric and P-E characteristics of ferroelectric devices are evaluated and interpreted.

- Exploration of a means to fabricate a transparent ferroelectric capacitor is initiated. Both transparent contacts alone and transparent contacts with the inclusion of an insulating buffer layer are investigated. Of the two buffer layer materials investigated for this thesis, CaF_2 shows better characteristics, including a high effective dielectric constant and moderate breakdown properties.

5.2 Recommendations for future work

This section contains recommendations for continuing this project. Experiments which may improve the crystallinity or transparency of PZT films are suggested. Recommendations for continuing the investigation of transparent contacts and transparent insulating buffer layers are provided. Lead-free ferroelectric materials are discussed.

5.2.1 Improved quality of PZT films

The quality of the PZT films used in the capacitors for this thesis may be improved by using slow furnace anneal in an oxygen ambient rather than the 650°C RTP.

Dielectric and polarization properties as well as crystal structure might be improved by altering the Zr/Ti ratio in the film. This is easily accomplished in CSD methods by altering the relative amounts of the Zr and Ti precursors in the solution.

Higher Zr content might improve leakage properties because $PbZrO_3$ has a lower electron affinity than $PbTiO_3$, which provides a more effective barrier to electron injection. $PbZrO_3$ is an antiferroelectric, so a very high Zr concentration should be avoided, since it might result in a double hysteresis loop as is characteristic of an antiferroelectric. [12]

Crystallinity might be engineered by spinning a thin layer of $PbTi0_3$ onto the substrate and annealing it before PZT is applied. $PbTiO_3$ forms the perovskite phase at temperatures as low as 400°C. [17, 21] Subsequent coats of PZT should form the perovskite phase on the $PbTiO_3$ layer. A solution for $PbTiO_3$ could be made from the precursors of the PZT solution.

The spin-coated films used in this thesis have surface texture which is a result of the spinning action. Waves form in the final films which are up to 10 nm in height. This effect is decreased when thinner (more dilute) solutions are used in the spinning and may be further improved by altering the spinning and drying times, as discussed in Ch. 4. Making films of many thin coats would reduce the surface texture, but care would have to be taken that particles are not incorporated into the film during the process. One of the biggest sources of particles is in the firing furnace due to the insulation in the furnace falling off the walls. If films are fired in a cleaner environment, either in a container within the furnace or in a different furnace, thinner coats could be used, and yield would improve.

The major advantage of limited surface texture would be that insulating buffer layers which my be required for transparent capacitors, could be made thinner, so that their effect on the capacitor dielectric constant and polarization are minimized.

Yield would also be improved by making the capacitors smaller. Smaller capacitors can be made using photolithography techniques. However, analysis tools such as the Sawyer-Tower circuit for P-E assessment would have to be modified in order to characterize smaller capacitors.

5.2.2 Transparent ferroelectric capacitors

As is evident from this thesis, transparent ferroelectric capacitors are difficult to fabricate. One aspect of transparency which has not been explored completely is the transparency of the ferroelectric film itself. The PZT films used in this thesis have a slight yellow tint. Optical transparency in PZT is improved with the incorporation of La dopants. [14, 18] PZT doped with lanthanum (PLZT) is discussed in Ch. 2 of this thesis. Imprint and fatigue problems are also reduced with the incorporation of La.

Preliminary solutions of PLZT have already been made in the OSU EECS solid-state materials processing laboratory. An experiment to determine optimal lanthanum doping for optical transparency and ferroelectric properties would be useful for fabricating transparent ferroelectric capacitors.

Insulating buffer layers of CaF_2, HfO_2, or other insulators may be required for the fabrication of transparent ferroelectric capacitors. Preliminary work using a CaF_2 buffer layer results in capacitors which exhibit ferroelectric behavior. If the PZT or PLZT films can be made smoother (less surface texture) it will be possible to deposit thinner insulating buffer layers. CaF_2 is currently the best available buffer layer choice because it is deposited by thermal evaporation, a process which is compatible with PZT. A high quality CaF_2 film on a high quality PZT film should yield a transparent ferroelectric capacitor.

HfO_2 is deposited at OSU by RF sputtering at a substrate temperature of 250°C. Both the substrate temperature under vacuum and the sputter-induced damage are likely to degrade the ferroelectric properties of the PZT. Spin-coating solutions to make high-quality HfO_2 are in development at OSU and may provide another means of fabricating transparent ferroelectric capacitors.

5.2.3 Transparent ferroelectric memories

In order to fabricate a transparent FRAM, a fully transparent ferroelectric capacitor must be fabricated and integrated with transparent thin film transistors. The integration issues include process compatibility and patterning of the ferroelectric layer. For process compatibility, the PZT layer cannot be exposed to thermal processes in reducing atmospheres or sputter ions without incurring damage and loss of ferroelectric properties. To pattern PZT, preliminary experiments with chemical and reactive ion etching have been performed, and reactive ion etching seems to be the most effective method.

To fabricate a transparent FEFET, process compatibility and gate leakage must be considered. For a top-gate device, for which the ferroelectric layer is deposited on the channel layer, the thermal processing for the ferroelectric layer must be safe for the underlying layers. Also, the ferroelectric material must be able to form the ferroelectric phase on the underlying layer. For a bottom-gate device, for which the channel and source and drain are deposited on the ferroelectric layer, the ferroelectric layer cannot be exposed to thermal processing in a reducing atmosphere or to sputter ions. Gate leakage current in bottom-gate FEFETs fabricated at OSU was higher than the source-drain current, making transistor properties impossible to determine. The inclusion of an insulating buffer layer should reduce gate leakage.

5.2.4 Other ferroelectric materials

Integrated circuit and electronics manufacturers are trying to remove Pb from all products by 2006. Other ferroelectric materials, such as SBT and BST, as discussed in Ch. 2, should be investigated for transparent ferroelectric applications. BST has similar processing parameters (e.g. temperature) to PZT, and lower leakage properties, but also a lower dielectric constant and lower remnant polarization. [25] SBT has a wide band gap (4.1 eV) and a similar electron affinity to PZT. A distinct disadvantage of SBT is that it requires a high processing temperature (750-800°C);

other than this, it seems to be a good replacement for PZT in transparent ferroelectric applications. [25]

5.2.5 Conclusions

In searching for materials for use in transparent ferroelectric applications, several things must be considered. An ideal transparent ferroelectric material is lead-free. It forms in the ferroelectric phase at low temperatures. Ferroelectric materials and contact materials must be chosen so that the band alignment inhibits leakage due to charge injection, or a transparent high dielectric constant insulating buffer layer must be employed to prevent charge injection. Also bulk current leakage properties should be minimized.

BIBLIOGRAPHY

1. M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectrics and Related Materials*. New York: Oxford University Press, 1977.

2. Y.-M. Chiang, D. P. B[irnie], and W. D. Kingery, *Physical Ceramics*. John Wiley and Sons, Inc., 1997.

3. J. F. Scott, *Ferroelectric Memories*. Berlin, New York: Springer, 2000.

4. B. A. Strukov and A. P. Lavanyuk, *Ferroelectric Phenomena in Crystals*. Springer, 1998.

5. T. Tybell, C. H. Ahn, and J. M. Triscone, "Ferroelectricity in thin pervoskite films," *Appl. Phys. Lett.*, vol. 75, pp. 856–858, August 1999.

6. P. Ghosez and K. M. Rabe, "Microscopic model of ferroelectricity in stress-free $PbTiO_3$ ultrathin films," *Appl. Phys. Lett.*, vol. 76, pp. 2767–2769, May 2000.

7. C. B. Sawyer and C. H. Tower, "Rochelle salt as a dielectric," *Physical Review*, vol. 35, pp. 269–275, February 1930.

8. J. T. Evans and J. A. Bullington, "A ferroelectric capacitor simulation model," in *1990 IEEE 7th International Symposium on Applications of Ferroelectrics*, (New York), pp. 692–697, IEEE, IEEE, 1991.

9. Q. Zhang, R. W. Whatmore, Z. Huang, and M. E. Vickers, "Low temperature formation of sol-gel derived ferroelectric lead zirconate titanate ($Pb(Zr_xTi_{1-x})O_3$, x=0.3) thin films," *J. Phys. IV France*, vol. 8, pp. 79–82, 1998.

10. P. W. Peacock and J. Robertson, "Band offsets and Schottky barrier heights of high dielectric constant oxides," *J. Appl. Phys.*, vol. 92, pp. 4712–4721, October 2002.

11. C. Kittel, *Introduction to Solid State Physics*. Hoboken, New Jersey: John Wiley and Sons, Inc, 7th ed., 1996.

12. L. B. Kong and J. Ma, "Preparation and characterization of antiferroelectric PLZT 2/95/5 thin films via a sol-gel process," *Mat. Lett.*, vol. 56, pp. 30–37, September 2002.

13. E. G. Lee, J. K. Lee, J.-Y. Kim, J. G. Lee, H. M. Jang, and S. J. Kim, "Zr/Ti ratio dependence of the deformation in the hysteresis loop of $Pb(Zr,Ti)O_3$ thin films," *J. Mater. Sci. Lett.*, vol. 18, pp. 2025–2028, 1999.

14. N. W. Jang, S. B. Mah, D. S. Paik, H. W. Choi, and C. U. Park, "Structural and electrical properties of PLZT films on ITO-coated glass prepared by a sol-gel process," *Mat. Res. Bul.*, vol. 34, no. 9, pp. 1463–1472, 1999.

15. S. Aggarwal and R. Ramsesh, "Point defect chemistry of metal oxide heterostructures," *Annu. Rev. Mater. Sci.*, vol. 28, pp. 463–499, 1998.

16. R. Thomas, S. Mochizuki, T. Mihara, and T. Ishida, "Effect of substrate temperature on the crystallization of $Pb(Zr,Ti)O_3$ films on Pt/Ti/Si substrates prepared by radio frequency magnetron sputtering with a stoichiometric oxide target," *Mat. Sci. & Eng. B*, vol. 95, pp. 36–42, 2002.

17. C. Vijayaraghavan, T. C. Goel, and R. G. Mendiratta, "Structural and electrical properties of sol-gel synthesized PLZT thin films," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 6, pp. 69–72, February 1999.

18. G. Yi, Z. Wu, and M. Sayer, "Preparation of $Pb(Zr,Ti)O_3$ thin films by sol-gel processing: Electrical, optical and electro-optic properties," *J. Appl. Phys.*, vol. 64, pp. 2717–2724, September 1988.

19. J. F. Wager, "Thermodynamics and kinetics of vacancy self-compensation in wide-bandgap semiconductors," *Philos. Mag. A*, vol. 67, no. 4, pp. 897–904, 1993.

20. T. Myers, P. Banerjee, S. Bose, and A. Bandyopadhyay, "Layered lead zirconate titanate and lanthanum-doped lead zirconate titanate ceramic thin films," *J. Mater. Res.*, vol. 17, pp. 2379–2385, September 2002.

21. G. Vélu, B. Jaber, T. Haccart, and D. Rèmiens, "Influence of $PbTiO_3$ buffer layer on structural properties of $Pb(Zr,Ti)O_3$ thin films produced by sputter deposition technique," *J. Phys. IV France*, vol. 8, pp. 243–246, 1998.

22. K. Yamakawa, K. Imai, O. Arisumi, T. Arikado, M. Yoshioka, T. Owada, and K. Okumura, "Novel $Pb(Zr,Ti)O_3$ (PZT) crystallization techique using flash lamp for ferroelectric RAM (FeRAM) ambedden LSIs and one transistor type FeRAM devices," *Jpn. J. Appl. Phys.*, vol. 41, pp. 2630–2634, 2002.

23. H. Ishiwara, *Handbook of Thin Film Devices, Volume 5: Ferroelectric Thin Film Devices*, ch. 3, pp. 79–89. Academic Press, 2000.

24. J. F. Scott, "High-dielectric constant for dynamic random access memories (DRAM)," *Annu. Rev. Mater. Sci.*, vol. 28, pp. 79–100, 1998.

25. A. I. Kingon and S. K. Streiffer, "Ferroelectric films and devices," *Curr. Opin. Sol. St. & Mat. Sci.*, vol. 4, pp. 39–44, 1999.

26. J. F. Scott and A. J. Hartman, "Effects of constrained geometries and fast access times in real ferroelectric memory devices," *J. Phys. IV France*, vol. 8, pp. 3–15, 1998.

27. D. J. Wouters, R. Nouwen, G. J. Norga, A. Bartic, L. V. Poucke, and H. E. Maes, "Switching quality of thin-film PZT ferroelectric capacitors," *J. Phys. IV France*, vol. 8, pp. 205–208, 1998.

28. B.-G. Yu, I.-K. You, W.-J. Lee, S.-O. Ryu, K.-D. Kim, S.-M. Yoon, S.-M. Cho, N.-Y. Lee, and W.-C. Shin, "Device characterization and fabrication issues for ferroelectric gate field effect transistor device," *J. Semicond. Tech. and Sci.*, vol. 2, pp. 213–224, September 2002.

29. S.-M. Yoon, E. Tokumitsu, and H. Ishiwara, "Ferroelectric neuron integrated circuits using $SrBi_2Ta_2O_9$-gate FET's and CMOS Schmitt-trigger oscillators," *IEEE Trans. Electron Devices*, vol. 47, pp. 1630–1635, August 2000.

30. H. N. Al-Shareef, K. R. Bellur, O. Auciello, and A. I. Kingon, "Phase evolution and annealing effects on the electrical properties of $Pb(Zr_{0.53}Ti_{0.47})O_3$ thin films with RuO_2 electrodes," *Thin Solid Films*, vol. 256, pp. 73–79, 1995.

31. B. Nagaraj, S. Aggarwal, and R. Ramesh, "Influence of contact electrodes on leakage characteristics in ferroelectric thin films," *J. Appl. Phys.*, vol. 90, pp. 375–382, July 2001.

32. I.-D. Kim and H.-G. Kim, "Characterization of highly-preferred $Pb(Zr,Ti)O_3$ thin films on $La_{0.5}Sr_{0.5}CoO_3$ and $LaNi_{0.6}Co_{0.4}O_3$ electrodes prepared at low temperature," *Jpn. J. Appl. Phys.*, vol. 40, pp. 2357–2362, 2001.

33. A. V. Rao, S. Mansour, and A. L. Bement, "Fabrication of ferroelectric PZT thin film capacitors with indium tin oxide ITO electrodes," *Mat. Lett.*, vol. 29, pp. 255–258, December 1996.

34. Y. Ohya, Y. Tanaka, and Y. Takahashi, "Dielectric properties of lead zirconate titanate thin film fabricated on In_2O_3:Sn substrate by sol-gel method," *Jpn. J. Appl. Phys.*, vol. 32, pp. 4163–4167, September 1993.

35. S. M. Sze, *Physics of Semiconductor Devices*. John Wiley and Sons, 1981.

36. O. Lang, C. Pettenkofer, J. F. Sanches-Royo, A. Segura, A. Klein, and W. Jaegermann, "Thin film growth and band lineup of In_2O_3 on the layered semiconductor InSe," *J. Appl. Phys.*, vol. 86, pp. 5687–5691, November 1999.

37. R. Mollers and R. Memming *Ber. Bunsenges. Phys. Chem.*, vol. 76, 1972.

38. M. Dawber and J. F. Scott, "Modelling of leakage current in ferroelectric thin film capacitors," *Ferroelectrics*, vol. 260, pp. 143–148, 2001.

39. Y. T. Kim and D. S. Shin, "Memory window of $Pt/SrBi_2Ta_2O_9/SiO_2/Si$ structure for metal ferroelectric insulator semiconductor field effect transistor," *Appl. Phys. Lett.*, vol. 71, pp. 2507–2509, December 1997.

40. S. Wolf, *Silicon Processing for the VLSI Era, Volume 2: Process Integration.* California: Lattice Press, 1990.

41. R. Ramesh, S. Aggarwal, and O. Auciello, "Science and technology of ferroelectric films and heterostructures for non-volatile ferroelectric memories," *Mat. Sci. & Eng.*, vol. 32, pp. 191–236, April 2001.

42. S. R. Summerfelt, *Thin Film Ferroelectric Materials and Devices*, ch. 1: (Ba,Sr)TiO_3 Thin Films For DRAMs. Kluwer Academic Publishers, 1997.

43. J. F. Scott and M. Dawber, "Physics of ferroelectric thin-film memory devices," *Ferroelectrics*, vol. 265, pp. 119–128, 2002.

44. T. P. Ma and J.-P. Han, "Why is non-volatile ferroelectric memory field-effect transistor still elusive?," *IEEE Trans. Electron Devices*, vol. 23, pp. 386–388, July 2002.

45. C. T. Black, C. Farrell, and T. J. Licata, "Supression of ferroelectric polarization by an adjustable depolarization field," *Appl. Phys. Lett.*, vol. 71, pp. 2041–2043, October 1997.

46. M. Takahashi, H. Sugiyama, T. Nakaiso, K. Kodama, M. Noda, and M. Okuyama, "Analysis and improvement of retention time of memorized state of metal-ferroelectric- insulator-semiconductor structure for ferroelectric gate FET memory," *Jpn. J. Appl. Phys.*, vol. 40, no. 4B, pp. 2923–2927, 2001.

47. H. Ota, H. Fujino, S. Migita, S.-B. Xiong, and S. Sakai, "All-perovskite-oxide ferroelectric memory transistor composed of $Bi_2Sr_2CuO_x$ and $Pb(Zr_{0.5},Ti_{0.5})O_3$ films," *J. Appl. Phys.*, vol. 82, pp. 8153–8158, June 2001.

48. S. Mathews, R. Ramesh, T. Venkatesan, and J. Benedetto, "Ferroelectric field effect transistor based on epitaxial perovskite heterostructures," *Science*, vol. 276, pp. 238–240, April 1997.

49. M. W. J. Prins, S. E. Zinnemers, J. F. M. Cillessen, and J. B. Giesbers, "Depletion-type thin-film transistors with a ferroelectric insulator," *Appl. Phys. Lett.*, vol. 70, pp. 458–460, January 1997.

50. S. Wolf and R. Tauber, *Silicon Processing for the VLSI Era, Volume 1: Process Technology.* California: Lattice Press, 2000.

51. D. L. Smith, *Thin-Film Deposition: Principles and Practice.* New York: McGraw Hill, 1995.

52. R. Hoffman, "Development, fabrication, and characterization of transparent electronic devices," Master's thesis, Oregon State University, 2002.

53. K. Amanuma, T. Mori, T. Hase, T. Sakuma, A. Ochi, and Y. Miyasaka, "Ferroelectric properties of sol-gel derived Pb(Zr,Ti)O_3 thin films," *Jpn. J. Appl. Phys.*, vol. 32, pp. 4150–4153, September 1993.

54. Y. J. Song, H. H. Kim, S. Y. Lee, D. J. Jung, B. J. Koo, J. K. Lee, Y. S. Park, H. J. Cho, S. O. Park, and K. Kim, "Integration and electrical properties of diffusion barrier for high density ferroelectric memory," *Appl. Phys. Lett.*, vol. 76, pp. 451–453, January 2000.

55. G. Yi, Z. Wu, M. Sayer, C. Jen, and J. F. Bussiere, "Piezoelectric lead zirconate titanate coatings on metallic wires," *Electron. Lett.*, vol. 25, pp. 907–908, July 1989.

56. J. P. Bender, "SPICE modeling of ACTFEL devices and OLEDS," Master's thesis, Oregon State University, June 2000.

57. A. M. Alper, ed., *Phase Diagrams in Advenced Ceramics*. Academic Press, 1995.

58. D. Adler and J. Feinleib, "Electrical and optical properties of narrow-band materials," *Phys. Rev. B: Condens. Matter*, vol. 2, pp. 3112–3134, October 1970.

59. Y. Ohya, T. Tanaka, and Y. Takahashi, "Dielectric poroerties of lead zirconate titanate thin film fabricated on In_2O_3:Sn substrate by sol-gel method," *Jpn. J. Appl. Phys.*, vol. 32, pp. 4163–4167, September 1993.

60. Y. Yang, Z. Chen, G. Zhao, and W. Zhang, "Structural and ferroelectric characterization of PZT thin films," *Int. J. Modern Phys. B*, vol. 16, no. 28 and 29, pp. 4460–4464, 2002.

61. B. A. Tuttle, *Thin Film Ferroelectric Materials and Devices*, ch. 6: Pb(Zr,Ti)O_3 Based Thin Film Ferroelectric Nonvolatile Memories. Kluwer Academic Publishers, 1997.

62. T. Minami, T. Miyata, and T. Yamamoto, "Work function of transparent conducting multicomponent oxide thin films prepared by magnetron sputtering," *Surface Coat. and Tech.*, vol. 108-109, pp. 583–587, 1998.